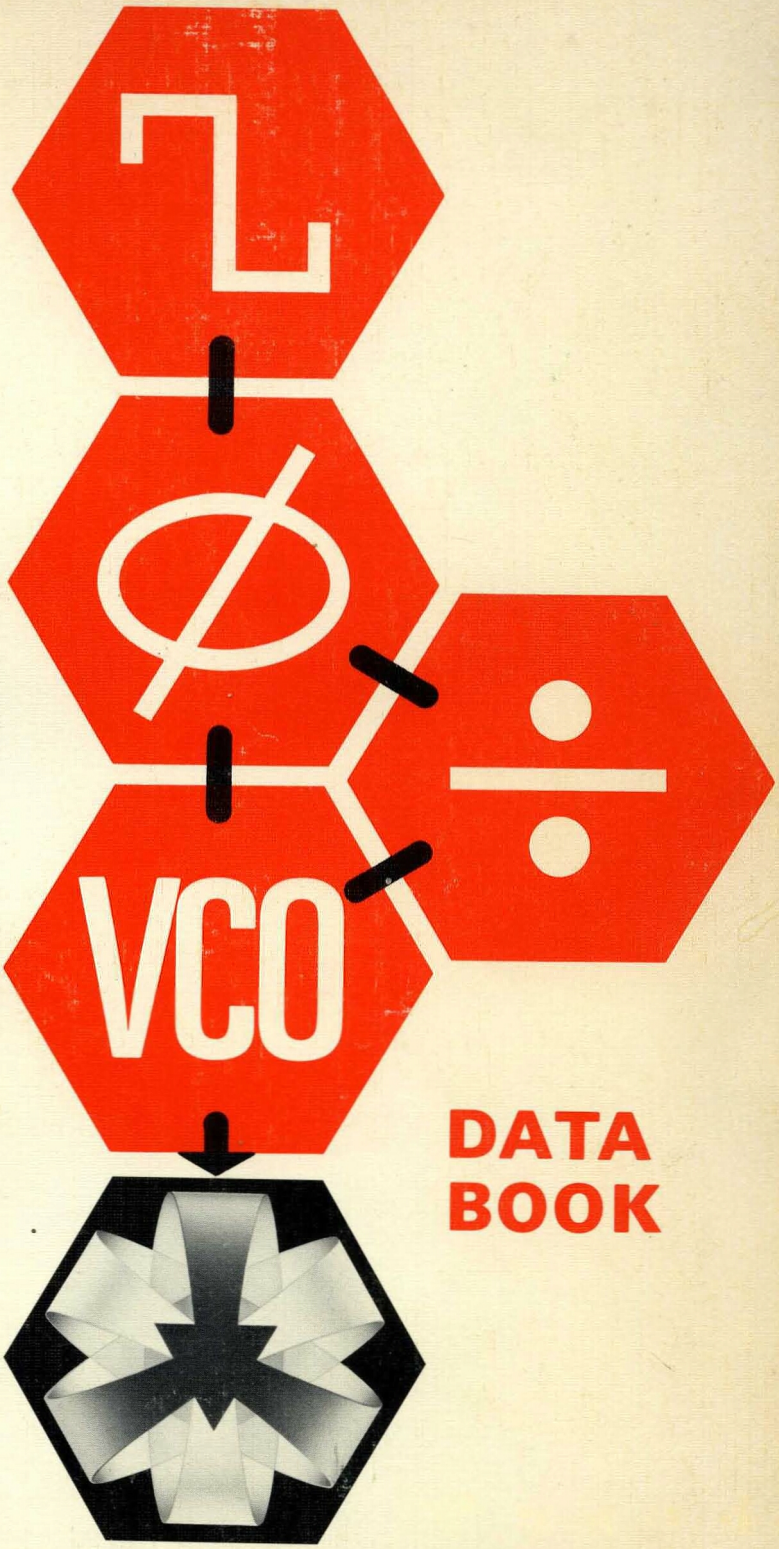
PHASE-LOCKED LOOP SYSTEMS



DATA BOOK

MOTOROLA Semiconductor Products Inc.

PHASE-LOCKED LOOP DATA BOOK

Second Edition
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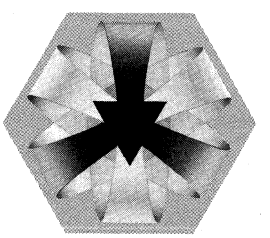

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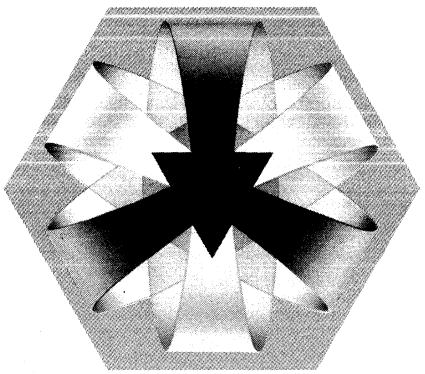


PURPOSE

What is presented here is a complete set of hardware that is used for the assembly of phase-locked loop frequency synthesizers. Each of the functions is compatible with its own logic family, as well as being capable of interfacing with other logic families through suitable translating circuits.

The circuits are optimized as independent entities rather than for a specific system, thereby increasing the system designer's flexibility. Equations for loop stability and bandwidth are discussed in the MC4344/4044 data sheet, and in application notes AN-532A and AN-535.

The new concepts presented are "digital harmonic mixing" and "digital phase detection". Harmonic mixing allows the generation of very high frequencies from one stable low frequency source. The system then need contain only one "tuned circuit" which is electronically variable and self aligning. Mixing itself requires no critical tank circuits and makes use of the narrow bandpass characteristics of the loop. Mixing can be combined with programmable counters or continuously-tuned oscillators to produce variable frequencies.

The digital phase detector's significance is its ability to discriminate both phase and frequency. The loop locks only on the fundamental and has a capture range limited only by the VCO range.

INTRODUCTION

Electronic phase locked loops (PLL) came into vogue in the 1930's when they were used for radar synchronization and communication applications. This technique for electronic frequency control is used today in satellite communication systems, airborne navigation systems, FM communication systems, computers, etc.

Motorola offers the designer a choice of specially designed integrated circuits for performing phase-locked loop functions: phase detection, frequency division, filtering, and voltage-controlled signal generation. This selection of functions permits the construction of reliable, high-performance loops of small size and low cost. In addition, the choice of circuits permits the designer to select TTL circuits where speed is not critical (<30 MHz), or ECL circuits where high speed is required (up to 500 MHz).

The circuits discussed are suitable for frequency synthesis, synchronization of digital signals, and clock recovery from encoded digital data streams.

The basic PLL technique compares the frequency and phase of the incoming data to the output of a voltage controlled oscillator (VCO). If the two signals differ in frequency and/or phase, an error voltage is generated and applied to the VCO, causing it to correct in the direction required for decreasing the difference. The correction procedure continues until lock is achieved, after which the VCO will continue to track the incoming signal.

These applications normally introduce two conflicting requirements: the system must very quickly lock-up to the incoming data and yet be capable of ignoring short term jitter inadvertantly introduced into the data. Using Motorola circuits, the required characteristics are established simply by selecting a few passive filter components. A typical application is discussed in more detail on the MC4344/4044 Phase-Frequency Detector data sheet.

One of the major applications of the PLL is frequency synthesis in the many systems which require discrete frequencies or fixed-channel spacing. For examples, the UHF television band (channels 14-83) extends from 470 MHz to 890 MHz in 6 MHz steps, and the aircraft VHF navigation/communication band is 108 MHz to 136 MHz in 25 KHz steps. AM and FM standard broadcast bands are also in channel form.

Motorola's integrated circuits lend themselves extremely well to frequency synthesizers. The remainder of this section is devoted to a description of Motorola PLL integrated circuits and their application to frequency synthesizers. Other applications are discussed on the individual data sheets (e.g., MC12012 included in this brochure).

Digital PLL Configurations

A number of frequency synthesizers that are tuneable in increments of a reference frequency, f_r, will be examined for economy and performance.

Direct PLL

Figure 1 is considered to be the direct approach. The output frequency is an integer multiple of the reference frequency ($f_{out} = N f_r$). This is the simplest form that the loop can assume but not necessarily the least expensive at higher frequencies. The VCO must be capable of operating at the output frequency. This is easily accomplished, up to 200 MHz. However, the complex programmable counters would also be required to operate at these frequencies. To achieve such speeds, special techniques or devices are required. Because high frequency (>25 MHz) programmable counters are expensive, special techniques to program the output frequency will now be discussed.

Multiplier PLL

In Figure 2, the input to the phase detector is f_r divided by 9, and the output of the VCO is multiplied by nine ($f_o = N \cdot f_r$). Since a lower effective reference frequency is employed, the response of the loop to a change in N is necessarily slower.

In addition, the output frequency is an integer multiple of the VCO frequency and this generally requires the use of tuned tank circuits. No problem is encountered if a fixed frequency or very small change in frequency is required. However, the multiplier tank must have high enough Q to multiply correctly, but low enough Q for sufficient bandwidth over the desired tuning range. From a manufacturing standpoint there are economic disadvantages: the tank must be tuned. This necessarily raises costs, and also creates a need for periodic servicing.

A final disadvantage caused by multiplying the VCO is that any perturbations in the VCO frequency are correspondingly multiplied. Sidebands which are sub-audio (below 300 Hz) at the VCO frequency may lie in the audible range after multiplication.

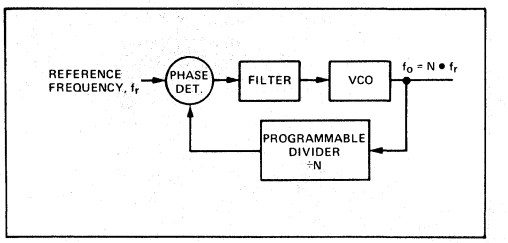


Figure 1 — Frequency Synthesis Using a Basic Phase-Locked Loop

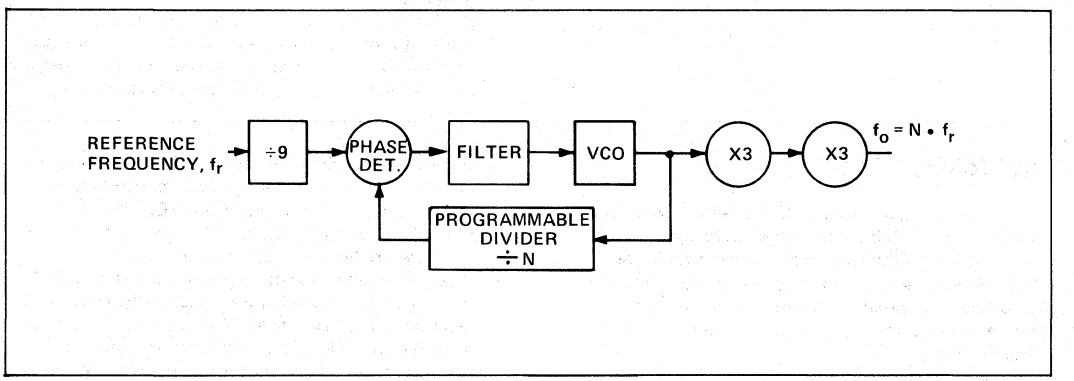


Figure 2 — Frequency Synthesis Using a Phase-Locked Loop and Output Multipliers

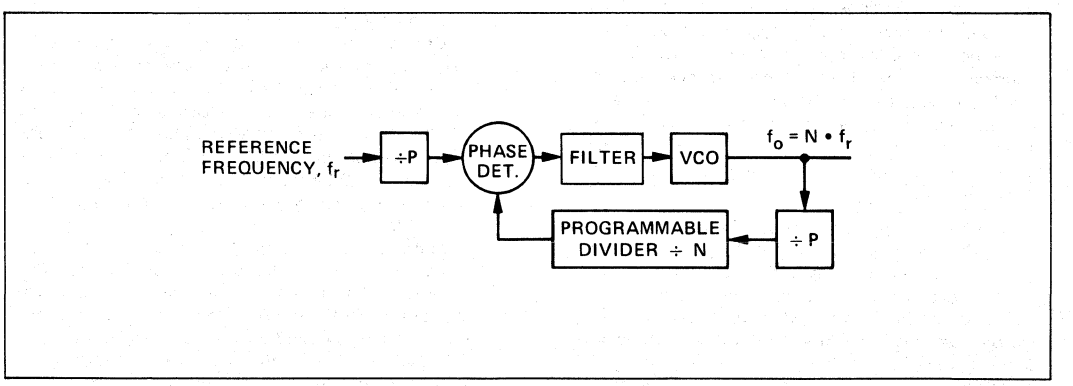


Figure 3 — Frequency Synthesis by Prescaling in the Phase-Locked Loop

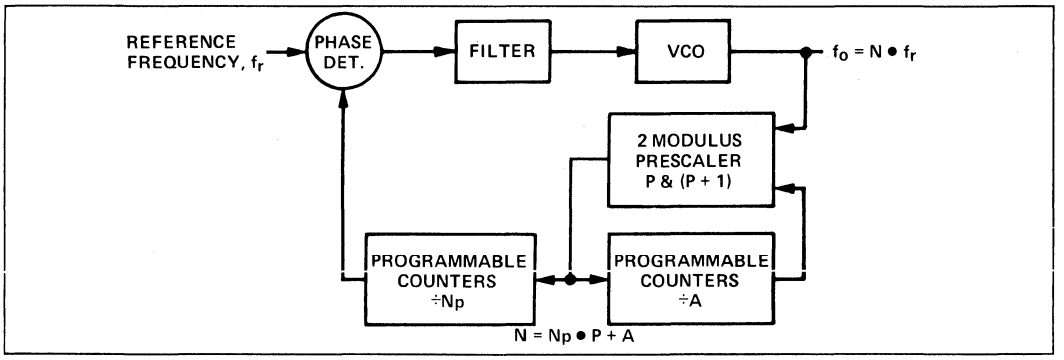


Figure 4 — Frequency Synthesis by Two Modulus Prescaling in the Phase-Locked Loop

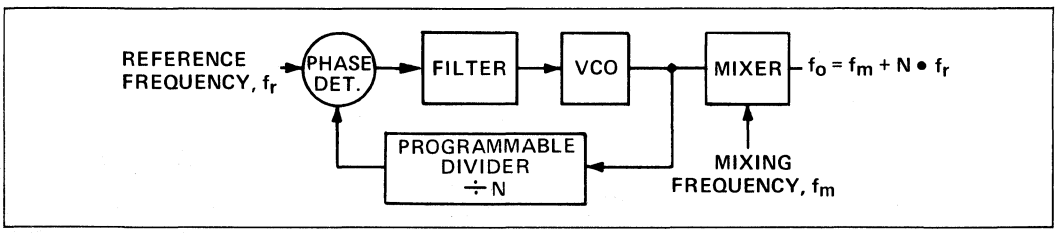


Figure 5 — Phase-Locked Loop Frequency Synthesis by Mixing Up

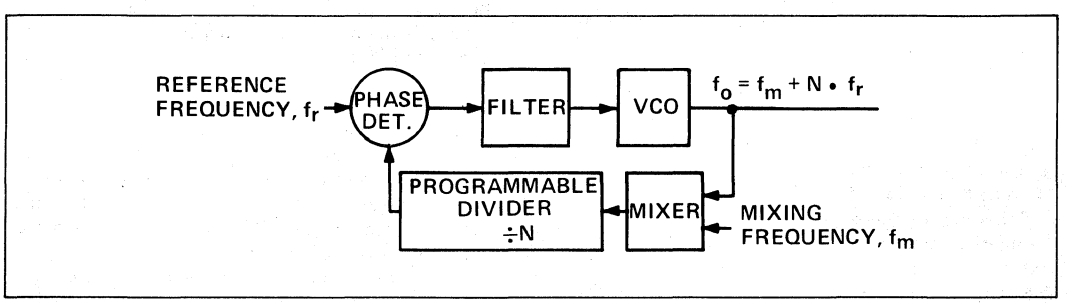


Figure 6 — Phase-Locked Loop Frequency Synthesis by Mixing Down

Prescaler PLL

The system shown in Figure 3 is somewhat better than that in Figure 2 since it places the frequency multiplication inside the loop. The VCO is now required to deliver substantially higher frequencies, but the tuned multipliers are eliminated. The prescaler block (÷ P) consists of a number of flip-flops connected as a fixed-divider chain. The input frequency into the divide by N is as low as that in Figure 2. Likewise, the loop response is slow.

Two Modulus Prescaled PLL

The configuration shown in Figure 4 includes a prescaler with provision for varying the modulus (divisor). Control is by means of a low frequency programmable counter. While the cost of this system is slightly greater than that shown in Figure 3, the performance is equal to that of the system in Figure 1.

PLL with Mixing Up

Figure 5 is a departure from the previous two system configurations. The reference frequency is equal to the channel spacing, and $f_o = f_m + N f_r$. This allows the VCO and logic a low operating frequency, but requires the generation of a fixed frequency (f_m) to mix to the higher frequency. It also requires a tuned output in the mixer, thus restricting the allowable tuning range.

PLL with Mixing Down

In Figure 6 the VCO is required to operate at the high output frequency. A mixing frequency, f_m, must be generated as a heterodyning signal and the mixer must be capable of handling the required input frequencies.

In this configuration, the mixer is placed inside the loop so that the effect of the mixing oscillator on the output frequency is included in loop action. As in Figure 5, $f_o = f_m + N f_r$.

PHASE-LOCKED LOOP COMPONENTS

1

Voltage Controlled Multivibrators — VCM (MC4024, MC1658)

The MC4024 and MC1658 voltage controlled multivibrators have output levels compatible with the TTL and ECL Families respectively. Both multivibrators have a typical tuning range of 4:1. The multivibrator sections of both devices are similar; therefore, the operation of only one will be described. For purposes of explanation, Figure 7 shows a somewhat simplified version of the multivibrator section of the MC1658.

In Figure 7, Q_1, Q_2, Q_5, R_1 and R_2 form a differential amplifier connected in a positive feedback configuration. Q_3, Q_4, Q_5, Q_6, R_1, R_2, R_3 and R_4 also form an amplifier connected for positive feedback. A common current source, I, is shared between the two amplifiers. The current I is divided between the amplifiers by means of Q_7, Q_8, and Q_9.

The basic oscillator section consists of the first amplifier (Q_1, Q_2, etc.) along with the timing capacitor, C, connected between the emitters of Q_1 and Q_2. In this configuration the charging current for C is I_1, and is controlled by Q_7 and Q_9.

The second amplifier (Q_3, Q_4, etc.) performs two major functions: 1) ensures proper and rapid switching of the multivibrator once the threshold voltage is reached; and 2) maintains a constant logic swing for the multivibrator over its entire tuning range. The latter helps maintain linear frequency-versus-voltage characteristics so desirable in voltage controlled multivibrators.

For a more detailed analysis of the operation of the multivibrator, consider the case when Q_2 and Q_3 have just turned on and Q_1 and Q_4 have turned off. The voltage across C at this time is $V\ell$ with the polarity as indicated in Figure 7. Since Q_1 and Q_4 are off, no current flows through R_1 and the voltage at the bases of Q_2 and Q_3 is (V_{CC} - V_{BE}). Since Q_2 and Q_3 are on, the current through R_2 is ($2I_1$ + I_2) and voltage of the bases of Q_1 and Q_4 is (V_{CC} - V_{BE} - R_2I). With Q_2 and Q_3 conducting, the voltage at point B is (V_{CC} - 2 V_{BE}), while at point A is the voltage at point B plus the voltage across C, or (V_{CC} - 2 V_{BE} + V). For this condition the voltage across the emitter-base junction of Q_1 is $\left[V_{CC} - V_{BE} - R_2I - (V_{CC} - 2V_{BE} + V\ell)\right] = V_{BE} - V\ell - R_2I$; the junction is reverse biased (assuming $V\ell + R_2I > V_{BE}$), and Q_1 is off.

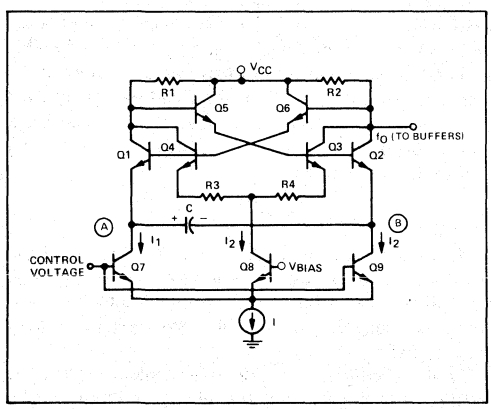


Figure 7 — Schematic of a Basic Voltage Controlled Multivibrator

With Q_1 and Q_4 off it can be seen that I_2 flows through Q_3 and $2I_1$ flows through Q_2. Since only I_1 can flow through Q_9, I_1 must flow through C to Q_7. Capacitor C starts charging from (V_{CC} - 2 V_{BE} + $V\ell$) toward V_{EE} at a rate equal to I/C. With point B held at a constant voltage of V_{CC} - 2 V_{BE}, the capacitor charges toward V_{EE} until point A reaches the threshold of Q_1, which is (V_{CC} - V_{BE} - R_2I).

Once the threshold voltage of Q_1 is reached, Q_1 starts to conduct. The current that flows through Q_1 causes a corresponding voltage drop across R_1. This voltage drop lowers the voltage at the emitter of Q_2. This voltage is transferred via C to drive point A lower and causes Q_1 to conduct more. In addition, as the current through Q_1 increases, a corresponding decrease in current through C and Q_2 occurs.

This decrease in current is reflected in a decrease of the voltage across R_2 which raises the voltage at the base of Q_1 causing further conduction.

At this point it becomes apparent that once the voltage at point A reaches the threshold of Q_1, the positive feedback of the circuit causes Q_1 to turn on rapidly and switch I_1 from C to R_1.

At some point during the switching of I_1 to the collector of Q_1, the increase in the voltage across R_1 and corresponding decrease in voltage across R_2 cause the voltages at the bases of Q_3 and Q_4 to enter the transition region of the differential amplifier, Q_3 and Q_4. Once the active region of the amplifier is reached, Q_4 begins to conduct. Due to the positive feedback connection for these transistors the same regeneration action occurs as described for Q_1 and Q_2, and I_2 is switched from Q_3 to Q_4.

After switching, Q_1 and Q_4 are on. Q_2 and Q_3 are off, the voltage across the capacitor is $V\ell = R_2I$ in a polarity opposite to the one indicated, and the voltage at point A is V_{CC} - 2 V_{BE}. The voltage at B is now V_{CC} - 2 V_{BE} + $V\ell$. One half cycle has been completed and the initial conditions stated are applied to the other half of the circuit. Ensuing operation is identical, and need not be discussed.

The differential amplifier (Q_3 and Q_4) plays an important role in the proper operation of the multivibrator. Resistors R_3 and R_4 must be made sufficiently large to ensure the multivibrator will enter the active region during the initial switching of either Q_1 or Q_2. However, the resistors cannot be made so large that they decrease the gain of the amplifier to less than 1. If either of these conditions are not met, the multivibrator will not function properly.

For a given value of C, the frequency of the multivibrator is varied by changing the charging current I_1 through the capacitor. I_1 is varied by

means of the steering network: Q_7, Q_8, and Q_9. Q_8 is tied to a fixed bias voltage, while Q_7 and Q_9 are connected to the control voltage input. As the control voltage is increased, I_1 through Q_7 and Q_9 increases and a corresponding decrease in I_2 occurs. As I_1 increases, C charges more rapidly and the frequency increases. From the previous discussion it may be noted that I_1 could be decreased to point where the $I_1 \cdot R_1$ drop would be insufficient to reach the active region of Q_3 and Q_4; then the multivibrator would cease to operate. Both the MC4024 and MC1658 have internal, non-varying current sources shunting Q_7 and Q_9 to ensure this condition does not happen.

Oscillator (MC1648)

An LC oscillator, (Figure 8), is sometimes preferable to an RC multivibrator because of the inherently higher Q of the frequency determining circuits. This results in lower noise. Switching oscillators (multivibrators) generally have poorer spectral purity.

The MC1648 is composed of an emitter-coupled pair of transistors, biased through the tank circuit to cause regeneration. Since a large voltage swing would forward bias the base collector junction of one transistor of this pair, an automatic gain control is added by means of an emitter-follower from the tank circuit. AGC action limits the swing to $E_{pp} = 2\pi R_E/R_C (V_{CC} - 2.2 V_{BE})$. A current source allows only enough current to flow so that this condition is met. In this circuit, component values were chosen to produce about a 500 mV peak-to-peak swing.

Since any additional load on the tank would decrease the Q of the oscillator and degrade spectral purity, a cascode transistor is used to couple from the emitter follower and to provide translation to a differential pair of transistors. These, in turn, produce a square wave compatible with existing ECL families. The output is highly buffered from the frequency determining components so that loading does not cause frequency shift.

Note that the tank circuit is approximately two diode drops above ground. This requires that the voltage on an external tuning mechanism be limited, or else capacitively isolated (see data sheet).

Programmable Counting (MC74416 and MC74418)

Although there are many ways to design programmable counters, only programmable-down counting will be discussed here. The operation is quite simple: a number is preset into the counter, the clock is enabled and the counter cycles to zero, at which time the number is preset again. The operation is slightly more complicated when several packages are connected together to form a larger counter. The necessary connections must be available to insure that the system behaves as a unified entity.

For an example, consider a modulus 10 counter. The truth table for its operation is shown in Figure 9. From any given number, the counter must cycle to

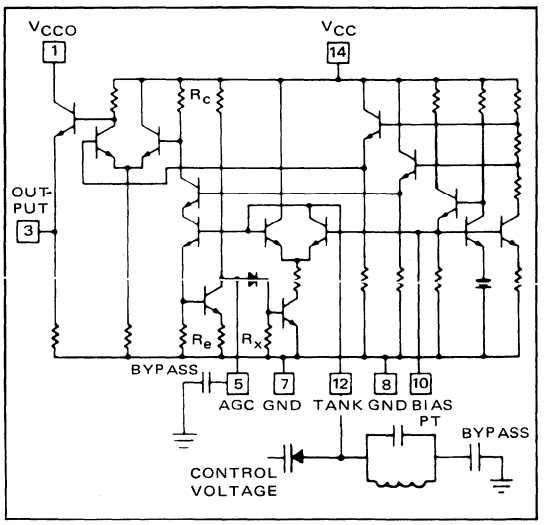


Figure 8 – ECO with MECL Output

CLOCKING TRANSITION Ø – 1

Q_8	Q_4	Q_2	Q_1
D	C	B	A
0	0	0	0
1	0	0	1
1	0	0	0
0	1	1	1
0	1	1	0
0	1	0	1
0	1	0	0
0	0	1	1
0	0	1	0
0	0	0	1
0	0	0	0

Figure 9 – Counter State Table

0000, and then if no preset information is applied, must return to 1001 (9) and count down again. A ripple counter can be used in this application since the most significant bits return to the zero state first. Operating speed is limited by the toggle rate of the least significant bit (or first flip-flop in the chain), and the logic required to detect the zero and preset conditions.

From an examination of Figure 9, it may be observed that the flip-flop to be used should change state on the positive going edge of the clock (transition from "Ø" to "1"). This may be accomplished with a D flip-flop if the $\bar{Q}$ output is returned to the D input. The first three flip-flops are connected in the normal ripple fashion, but the last flip-flop's clock is driven from the Q output of the first flip-flop.

To detect the 0000 state, the Q outputs from the second and third flip-flops are ANDed at the input to

the fourth flip-flop, and the inverted result is ANDed with the toggle feedback to the second flip-flop. Logic connections are shown in Figure 10. The result of these interconnections is the transition from 0000 to 1001.

The basic counter must be capable of being preset to a given number when the counts of all decades reach zero. To detect the zero states requires the AND of all $\overline{Q}$s (or equivalent logic). For practical reasons it is not convenient to build a fan-in gate to do this. Thus each decade provides the NOR function of the Q outputs through an "open collector" gate.

These outputs can be bussed or tied together with one common pull-up resistor as shown in Figure 11. All decades must have a 0 state (0000) if the output is to rise to a logic 1. It is this change in output level that effects preset of the programmed number.

The preset function is accomplished on each flip-flop in the manner shown in Figure 12. This operation must override the effects of the clock input.

Consider presetting to 0001 from 0000. If the preset did not suppress the clock the entire decade would ripple to 1111. This effect becomes more serious as the decades are cascaded. Also, it is desirable to have a predictable pulse width for the output frequency.

In the circuit of Figure 12, the output pulse width is equal to the pulse width of the input frequency. The reset pulse is inhibited until the 1 - Ø transition of the clock edge. This is accomplished by connecting the clock and gate inputs together as shown in the logic diagram of Figure 10. The clock and gate input, and bus output for a divide by 5 are shown in Figure 13.

Figure 11 also illustrates how several decades may be cascaded. To examine the cascade's operation, consider division by 497 (0100 1001 0111). The least significant decade is decremented first. When the first decade count reaches 0000, the next pulse clocks it to a 9 (1001) and decrements the second decade by one count. The result is now 0100 1000 1001.

The second decade continues to be decremented once for every 10 pulses into the first decade. The third decade responds to the second decade in the

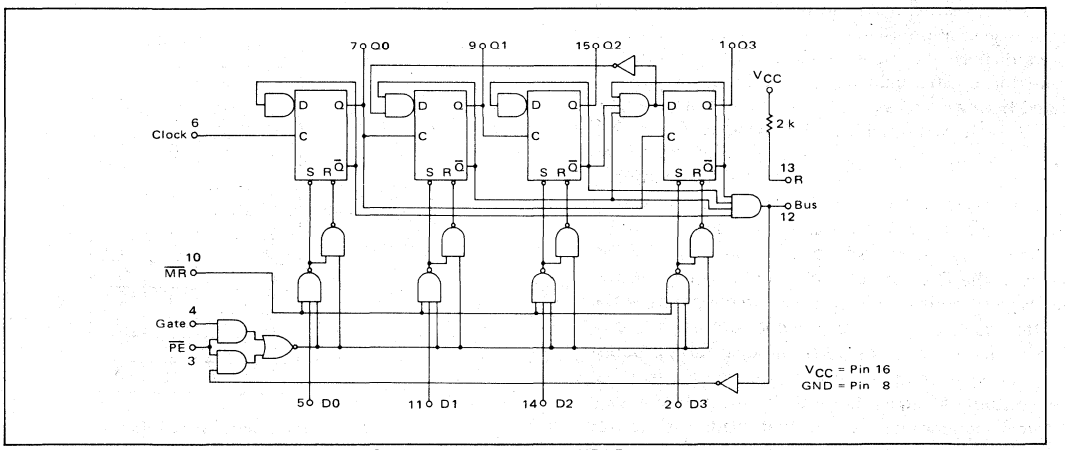


Figure 10 – Logic Diagram for an NBCD Programmable, Cascadeable, Divide By N Counter

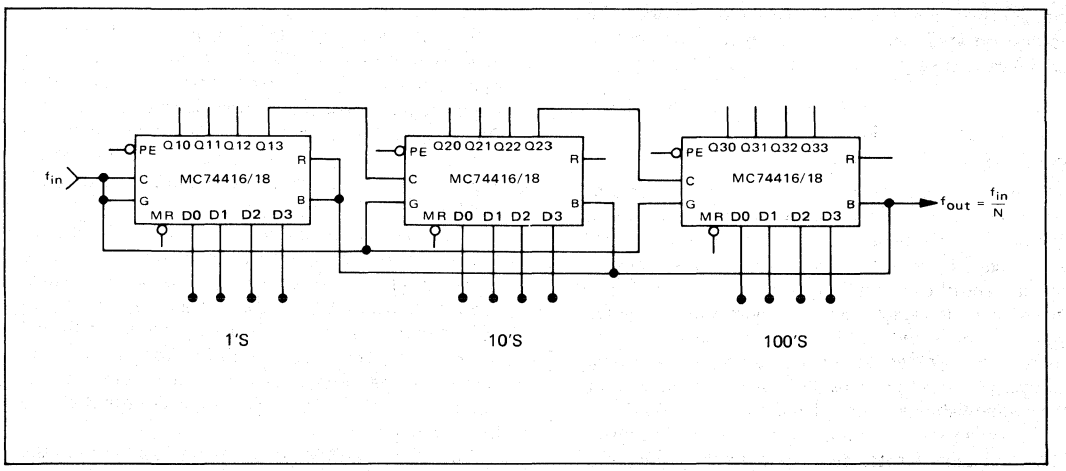


Figure 11 – 3 Stage Programmable Decade Frequency Divider

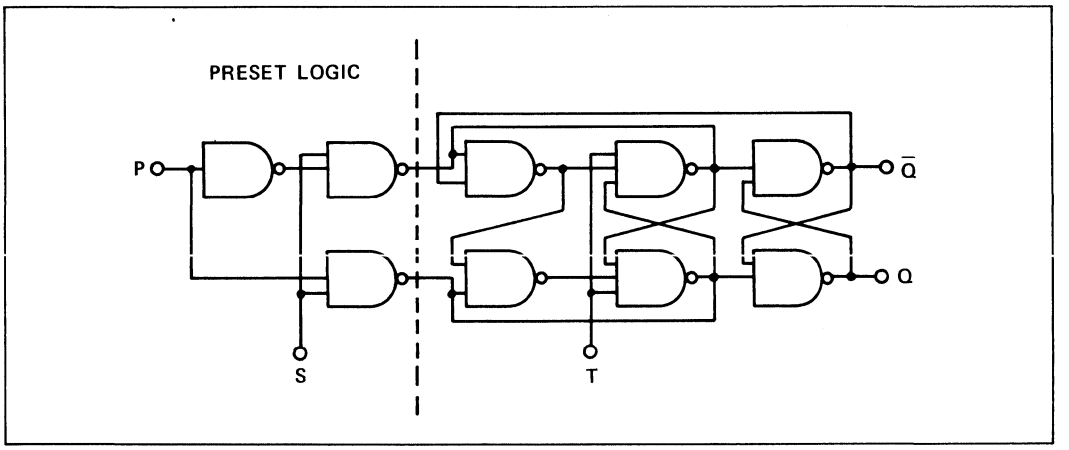


Figure 12 – Presettable Counter Logic Element

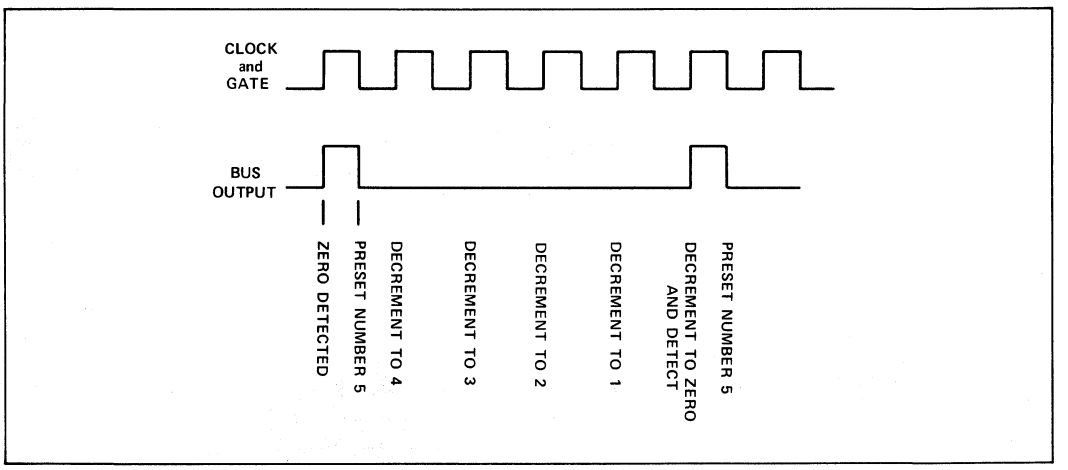


Figure 13 – Presettable Counter Timing Diagram

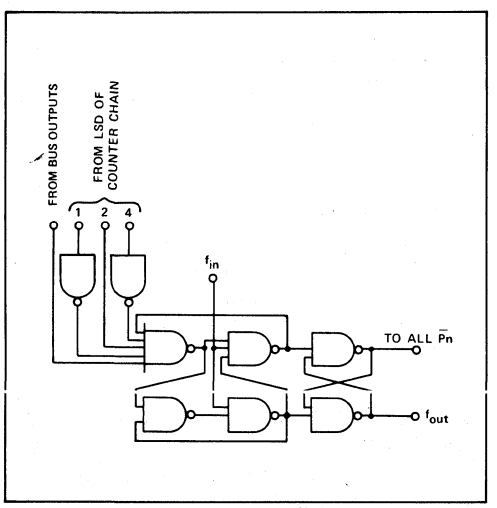


Figure 14 – Frequency Extender

same manner that the second decade responds to the first.

It is important to note that the preset information tells the counter only where to start and is not the modulus of the counter.

In some applications a binary counter has been substituted for the decade counter for division through 1599 instead of 999. This is allowable since the most significant decade counts down only once and does not recycle. It is useful to notice that the most significant decade returns to zero before the other decades, permitting cascading with no loss in operating speed of the input frequency.

In Figure 11, the counter may be built with TTL logic. While the toggle rate of the flip-flops used would be in excess of 30 MHz, the speed of the presettable counter altogether will only be about 8 MHz. This does not meet the requirements set forth originally. Consequently a look-ahead technique has been developed so that the counter can be operated in excess of 25 MHz. The technique is called "frequency extension".

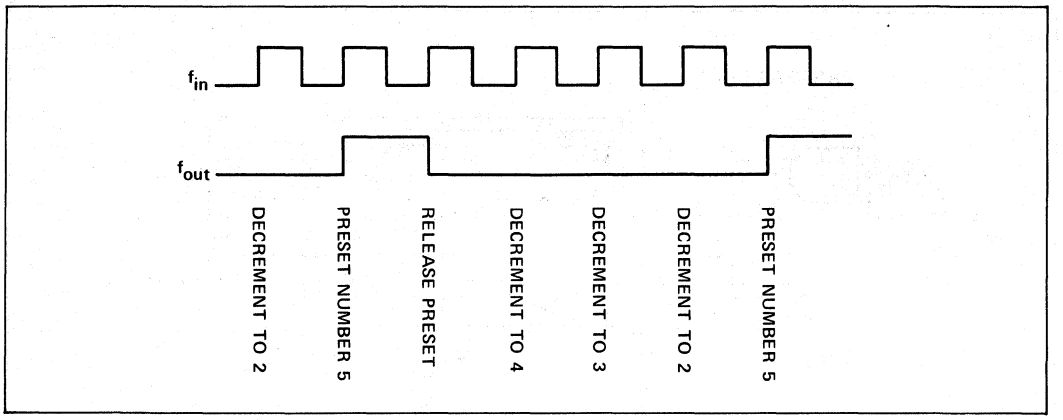


Figure 15 – Frequency Extender Timing Diagram

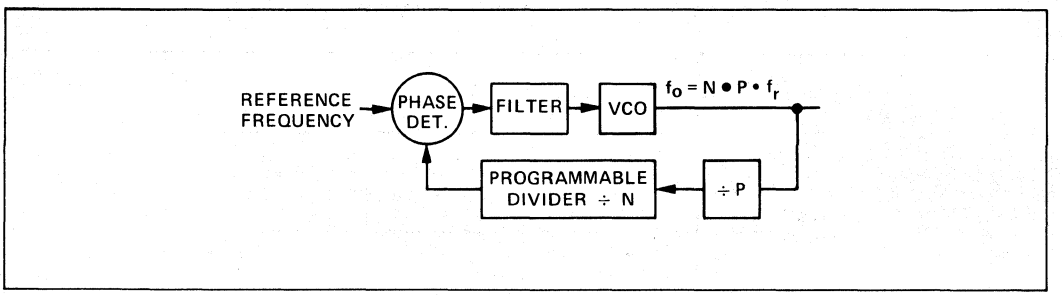


Figure 16 – Frequency Synthesis by Prescaling

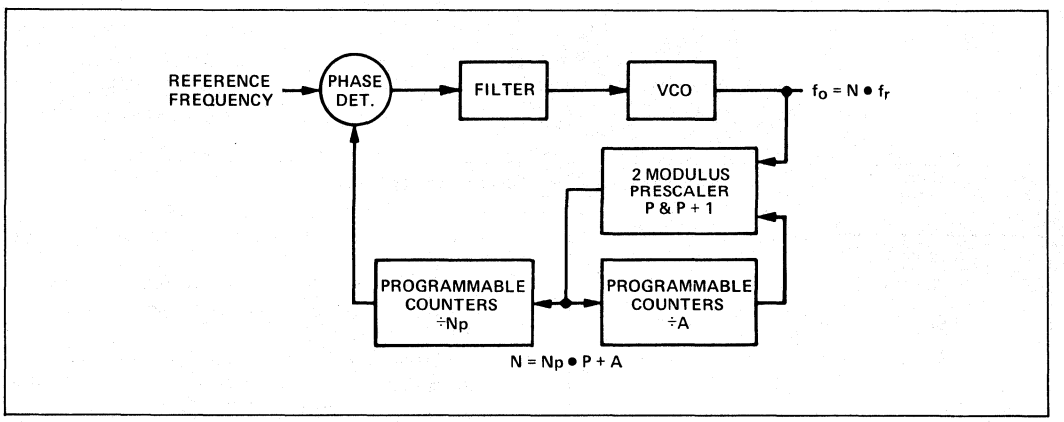


Figure 17 – Frequency Synthesis by Two-Modulus Prescaling

The frequency extender to be used consists of several gates connected to form a D flip-flop that detects the 0000. . . 0010 (2) state of the counter. The presets of the counter are activated on the first count and released on the zeroeth count. This logic is shown in Figure 14. The timing diagram and associated states are shown in Figure 15.

Notice that in Figure 13 the zero is detected after the clock makes a positive transition and the information is preset after the negative transition. This allows only half a cycle time for presetting as opposed to Figure 15 which allows a full cycle. Also, the minimum clock width necessary to establish the pulse width from the bus gate is eliminated. The combination of the two factors allows about a three-fold increase in operating speed. The output frequency can be taken from the output synchronous with the input.

The Technique Of Direct Programming By Utilizing A Two Modulus Prescaler (MC12012)

The disadvantage of using a fixed modulus (÷ P) for frequency division in high frequency phase-locked loops (cf Figure 16) is that it also requires

dividing the desired reference frequency by P (desired reference frequency equals channel spacing).

The MC12012 is specially designed for use with a technique called "variable modulus prescaling". This technique allows a simple MECL two-modulus prescaler (MC12012) to be controlled by a relatively slow MTTL programmable counter. The use of this technique permits direct high-frequency prescaling without any sacrifice in resolution since it is no longer necessary to divide the reference frequency by the modulus of the high frequency prescaler.

The theory of "variable modulus prescaling" may be explained by considering the system shown in Figure 16. For the loop shown:

$$f_{out} = NPf_{ref}, \quad (1)$$

where P is fixed, and N is variable. For a change of 1 in N, the output frequency changes by Pf_{ref}. If f_{ref} equals the desired channel spacing, then only every P channel may be programmed using this method. A problem remains: how to program intermediate channels.

One solution to this problem is shown in Figure 3. $A \div P$ is placed in series with the desired channel spacing to give a reference frequency: channel spacing/P.

Another solution is found by considering the defining equation (1) for f_{out} of Figure 16. From the equation it may be seen that only every P channel can be programmed simply, because N is always an integer. To obtain intermediate channels, P must be multiplied by an integer plus a fraction. This fraction would be of the form: A/P. If N is defined to be an integer number, Np, plus a fraction, A/P, N may be expressed as:

$$N = Np + A/P.$$

Substituting this expression for N in equation 1 gives:

$$f_{out} = (Np + A/P) \cdot P \cdot f_{ref}; \quad (2)$$

or:

$$f_{out} = (Np\,P + A) \cdot f_{ref}, \quad (3)$$

$$f_{out} = Np \cdot f_{ref} + A \cdot f_{ref}. \quad (4)$$

Equation 4 shows that all channels can be obtained directly if N can take on fractional values. Since it is difficult to multiply by a fractional number, equation 4 must be synthesized by some other means.

Taking equation 3 and adding ±AP to the coefficient of f_{ref}, the equation becomes:

$$f_{out} = (Np \cdot P + A + A \cdot P - A \cdot P)\, f_{ref}. \quad (5)$$

Collecting terms and factoring gives:

$$f_{out} = \left[(Np - A)\,P + A\,(P + 1)\right] f_{ref}. \quad (6)$$

From equation 6 it becomes apparent that the fractional part of N can be synthesized by using a two-modulus counter (P and P+1) and dividing by the upper modulus, A times, and the lower modulus, (Np - A) times.

This equation (6) suggests the circuit configuration in Figure 17. The A counter shown must be the type that counts from the programmed state (A) to the enable state, and remains in this state until divide by Np is completed in the programmable counter.

In operation, the prescaler divides by P+1, A times. For every P + 1 pulse into the prescaler, both the A counter and the Np counter are decremented by 1. The prescaler divides by P + 1 until the A counter reaches the zero state. At the end of (P+1) · A pulses, the state of the Np counter equals (Np - A). The modulus of the prescaler then changes to P. The variable modulus counter divides by P until the remaining count, (Np - A) in the Np counter, is decremented to zero. Finally, when this is completed, the A and Np counters are reset and the cycle repeats.

To further understand this prescaling technique, consider the case with P = 10. Equation 6 becomes:

$$f_{out} = (A + 10Np) \cdot f_{ref}. \quad (7)$$

If Np consists of 2 decades of counters then:

$Np = 10N_0 + N_1$ (N_0 is the most significant digit),

and equation 7 becomes:

$$f_{out} = (100\,N_0 + 10\,N_1 + A)\, f_{ref}.$$

Counter Control Logic (MC12014)

If the two-modulus prescaler is to operate at frequencies in excess of 200 MHz, then the counters following the prescaler must operate above 20 MHz (basic mode of operation of the prescaler being ÷ 10). The programmable counters have a maximum frequency of approximately 8 MHz without the frequency extender.

A circuit to control the variable modulus counter and extend the frequency of operation of the divide by Np and A counters is shown in Figure 18. Gates 1 through 8 form a latch which goes to a 1 state and remains there when a Ø appears on $\overline{Z}_0$, $\overline{Z}_1$, $\overline{Z}_2$ and $\overline{Z}_3$, and a 1 appears on B_2. The B_2 input is required only when more than 1 programmable counter is used for the ÷ A counter. Once set to a 1, the output of gate 8 remains at 1 regardless of the states appearing at inputs $\overline{Z}_0$, $\overline{Z}_1$, $\overline{Z}_2$, $\overline{Z}_3$ and B_2, and can be reset to Ø only by an input from the circuit comprised of gates 9 through 12. Gates 9 through 12 are used to determine the end of a divide cycle.

The output of the frequency extender is sampled on every positive transition of the clock input. When the output of the extender goes high signifying the end of a cycle, gates 9 through 12 are enabled and the latch is reset on the next positive transition of the clock. The operation of these parts may be further clarified by considering the complete system shown in Figure 19.

To understand the operation of the system shown in Figure 19, consider the case in which it is desired to divide by 43. This is accomplished by programming $N_0 = Ø$, $N_1 = 4$, and A = 3. The waveforms for various points in the circuit are shown in Figure 20 for this division.

From the waveforms it may be seen that the two-modulus prescaler starts in the ÷ 11 mode. The first pulse causes point A to go high. This positive transition decrements the upper counter to 3 and the

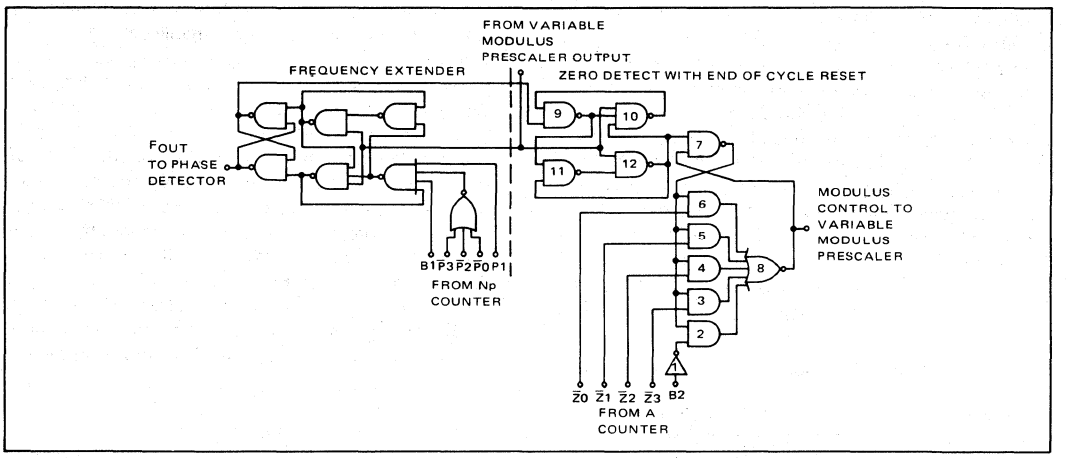


Figure 18 – Counter Control Logic

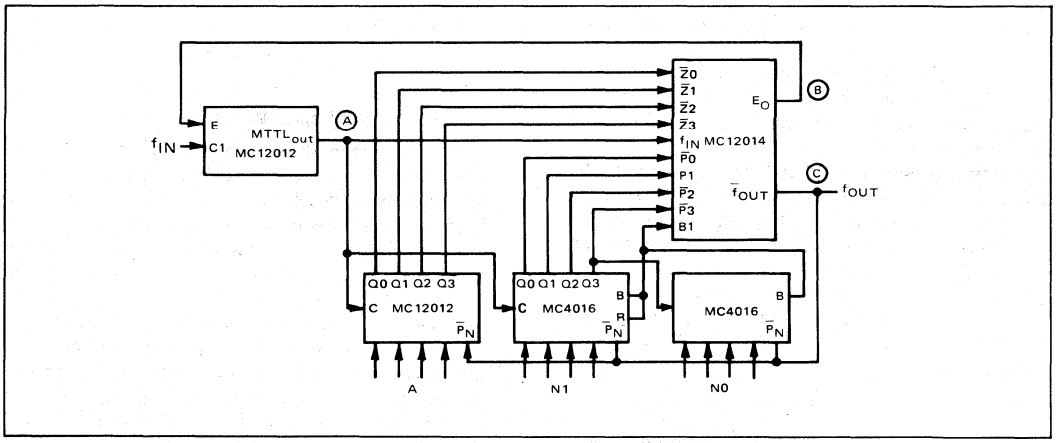


Figure 19 – Direct Programming Using a Two Modulus Prescaler

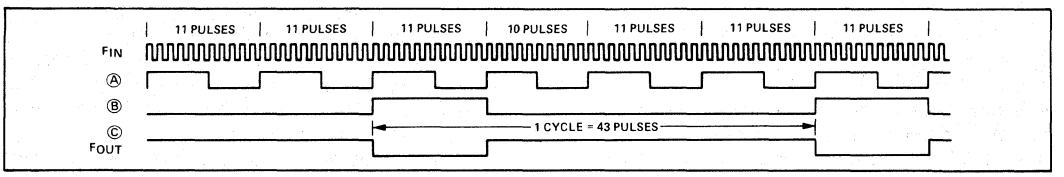


Figure 20 – Waveforms for Division by 43

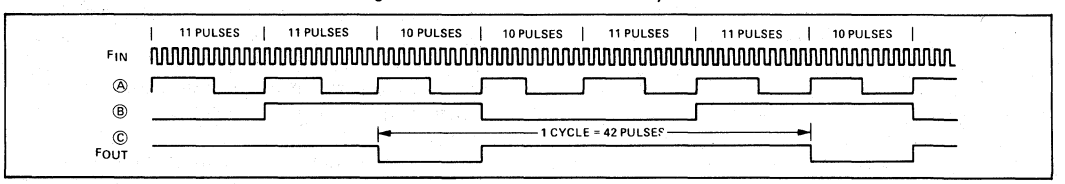


Figure 21 – Waveforms for Division by 42

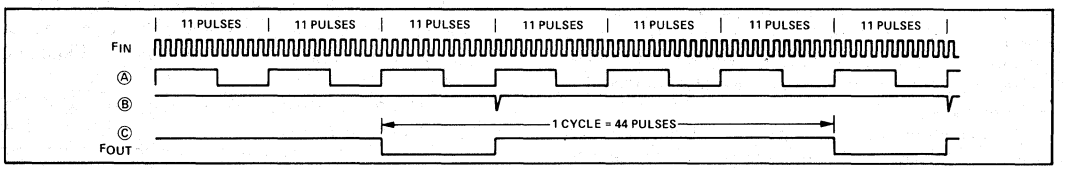


Figure 22 – Waveforms for Division by 44

lower counter to 2. After 11 pulses point A again goes high and decrements the upper counter to 2 and the lower counter to 1. The 2 contained in the upper counter enables the inputs to the frequency extender.

After 11 more pulses point A goes high again. With this positive transition, the output (f_{out}) of the extender goes low, the upper counter goes to 1, and the lower counter goes to Ø. Point B goes to 1 and will change the modulus to 10 at the start of the cycle. When f_{out} goes low, the programmable counters are reset to the programmed number. After 11 pulses (the enable went high after the start of the cycle and therefore doesn't change the modulus until the next cycle), point A makes another positive transition. This positive transition causes f_{out} to return high, releases the preset on the counters, and generates a pulse to clear the latch (return point B to Ø). After 10 pulses the cycle begins again (Point B was high prior to point A going high). The number of input pulses that have occurred for this operation is 3 X 11 + 10 = 43. Figures 21 and 22 show the waveforms for ÷ 42 and ÷ 44 respectively.

This method may be used in any application as long as the number in the Np counter is larger or equal to the number in the A counter. Failure to observe this rule will result in erroneous results. For example, for the system shown in Figure 20 if the number 45 is programmed the circuit will divide by 44.

Digital Mixing (MC12000)

The operation of the "D" flip-flop as a mixer may be understood if it is regarded as a binary zero-order-hold filter. If the input is a logic 1 when the clock makes its transition the output goes to and remains a 1 for a full clock period. If it were at a 1 from the previous time, it remains at a 1. The same is true for logic Ø inputs.

Of prime interest is the output frequency rather than the amplitude. The output "sequency" as a function of input frequency is shown in Figure 23. The word sequency is used to describe the output waveform, because the proper number of waveform edges occur per given length of time although they may not be evenly spaced. However, the filter in the loop can be adjusted to compensate for this. It is interesting to note the harmonic relation of the sampling frequency to the input and output functions. Figure 24 illustrates, for example, that the same output range can be achieved by using a mixing oscillator of one-half of the apparent mixing frequency. At this point it is of use to establish the

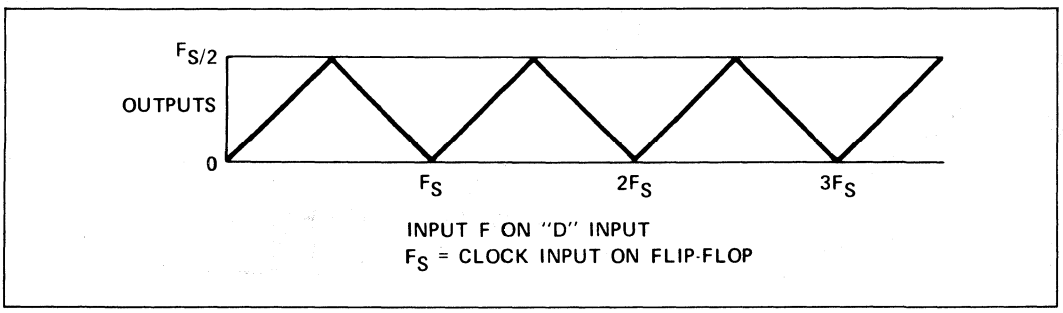


Figure 23 – Digital Mixer Transfer Function

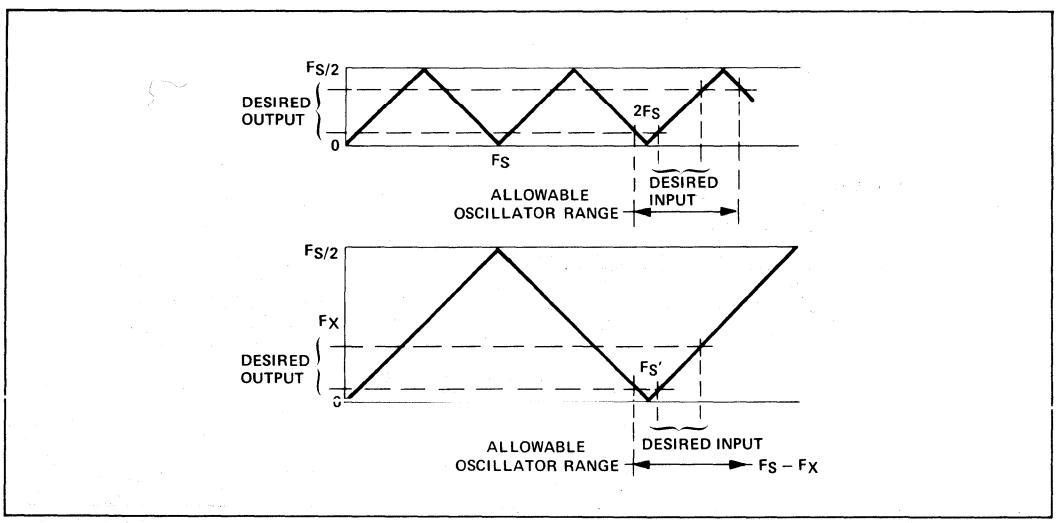


Figure 24 – Harmonic Mixing

configuration of a system to see how this technique can be extended. Such a system is shown in Figure 25.

The conversion of the high frequency signal to a low frequency signal has forced the generation of a local oscillator frequency. This should be generated with as few components as possible. Applying the previously mentioned technique, the eleventh harmonic (55 MHz) of a reference (5 MHz) is mixed with 56 MHz from the VCO. This produces 1 MHz, which is used as the feedback to lock onto the reference frequency 1 MHz.

It is evident from this illustration that when mixing of this sort is used, the range of the VCO could lock at 51 or 61 MHz. It would not lock at 54 MHz or 59 MHz since the slope is in the wrong direction, but the information at the phase detector causes the system to "hang up" at either the high or low end of the VCO's range.

Figure 26 shows the range of interest for the system of Figure 25. It can be seen that if the input frequency is slightly less than 54 MHz the output sequency is slightly greater than 1 MHz, so the loop responds by attempting to drive the VCO down in frequency. If the input frequency is slightly greater than 59 MHz, the output sequency is slightly less than 1 MHz, and the loop responds by trying to raise the VCO's frequency.

The VCO must therefore be restricted to operate above 54 MHz and below 59 MHz. This can be accomplished in a variety of ways: by the proper choice of a tuning diode with respect to the L and C values of the VCO tank; or by dc clamping of the input voltage to the VCO. Once the values are established with appropriate tolerances, this subsystem does not require alignment after assembly.

Of interest are the frequency spectra at various points in the circuit. Figure 27 shows the spectrum of the crystal oscillator. The shape of the curve in this case is determined by the analyzer. If the oscillator is delivering an absolutely pure sine wave the picture appears as shown.

Figure 28 shows the spectrum of the 56 MHz oscillator. Again, the limiting factor in observing the

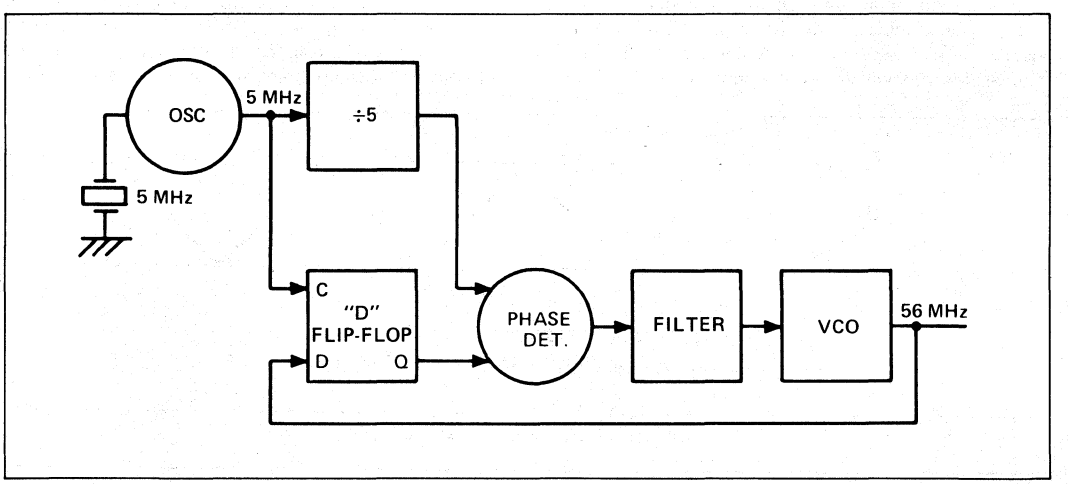


Figure 25 – Harmonic Mixing System

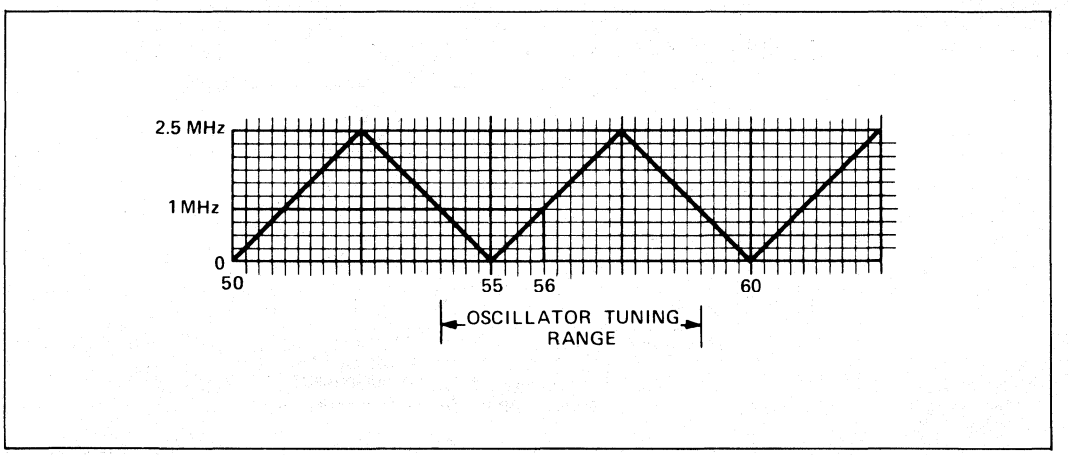


Figure 26 – Mixer Transfer Function

response is determined by the analyzer. It must be noted that while it is impossible to see exactly what the oscillator purity is, the output is down from the center frequency by at least 50 dB at plus or minus 300 Hz (considered the low end of the audio range useful for communication). The output from the mixer, Figure 29, is worth observing since the null at the 5 MHz sampling rate, as well as the 1 MHz peaks, can be seen.

To illustrate the continuity of the mixing action, consider the system shown in Figure 30. A tunable oscillator of 1 MHz is used as the reference input to a loop whose tuning range has been restricted to greater than 12 MHz and less than 14.75 MHz. The local oscillator frequency is 3.25 MHz which gives an apparent mixing frequency (4 X 3.25) of 12 MHz. Since the input oscillator is tunable, there is no guarantee of phase coherence between it and the crystal controlled reference oscillator.

Figures 31, 32, and 33 show the respective local oscillator, mixer output, and reference oscillator spectra. Since they are all on the same scale, a comparison reveals that nulls on the mixer are produced at the harmonics of the mixer frequency, and that the first maximum of the mixer output is coincident with the fundamental of the reference oscillator.

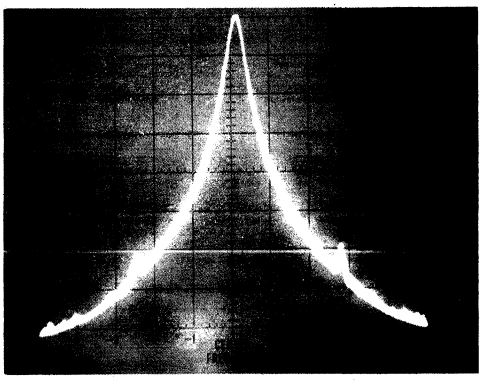
As the reference frequency is tuned from 1 MHz to 1.5 MHz (although it is not possible to measure at the infinite number of frequencies between these two limits and guarantee a one to one correspondence), no evidence of sporadic operation is noted. While the reference is swept, a frequency ratio counter connected at the inputs of the phase detector always measures 1.000000.

The gain constant of the mixer can be found by examining the change in output frequency with respect to input frequency. Examination of Figure 26 shows this to be plus or minus one, depending on the slope that the input frequency intersects. An experimental method of proving this is to put a step change of frequency into the reference input of the loop shown in Figure 30. The VCO is restricted to operate on several different slopes of the mixing curve and the filter response examined. In all cases the waveforms are identical.

Phase Detection (MC4044)

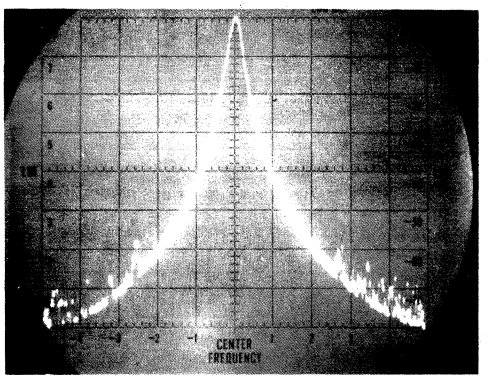
The phase detection system is perhaps the most important part of the system. Noise and sidebands present in the loop are directly related to the output amplitude and waveform. Prior systems have used analog multipliers as phase detectors in which the output contains sum and difference frequencies. The sum frequencies are filtered out, and the loop tries to reduce the difference frequency to zero.

A digital form of multiplier is an Exclusive-OR gate. In this application a symmetrical square wave at twice the reference frequency represents the locked condition. Phase error is represented by asymmetry in the output waveform. In both these systems, lock



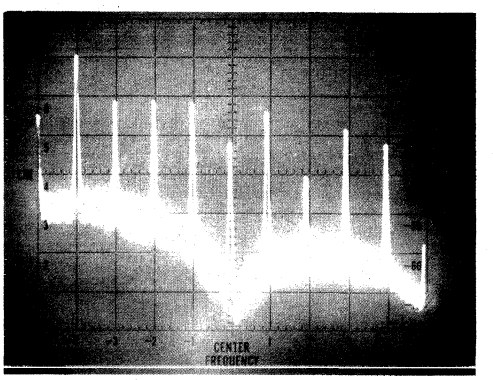
BANDWIDTH 50 Hz
SCAN WIDTH 200 Hz/cm
CENTER FREQUENCY 5 MHz

Figure 27 — Reference Oscillator Spectrum



BANDWIDTH 50 Hz
SCAN WIDTH 200 Hz/cm
CENTER FREQUENCY 56 MHz

Figure 28 — VCO Output Spectrum



BANDWIDTH 40 kHz
SCAN WIDTH 1 MHz/cm
CENTER FREQUENCY 5 MHz

Figure 29 — Mixer Output Spectrum

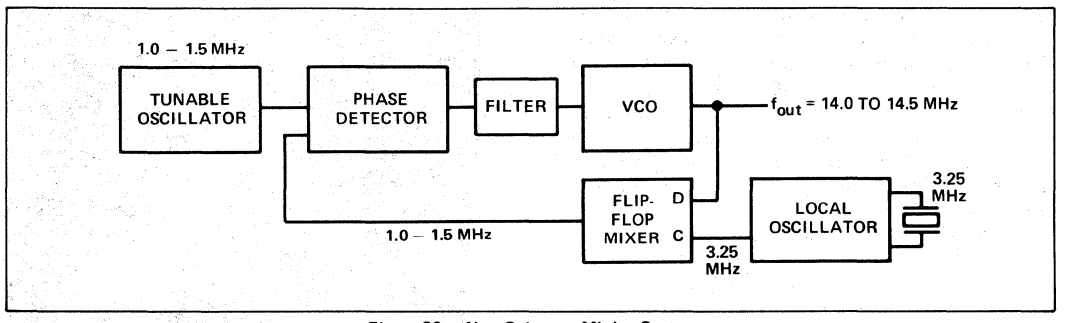
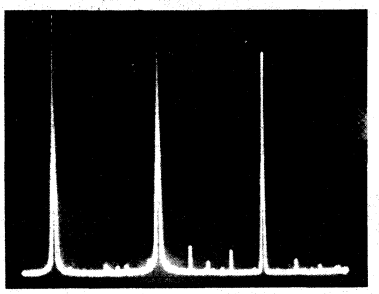
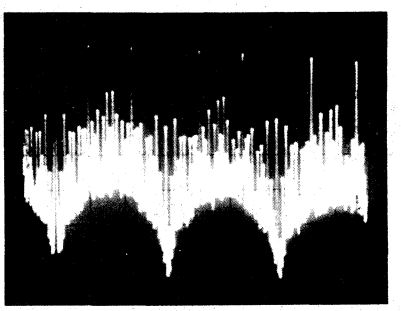


Figure 30 – Non-Coherent Mixing System



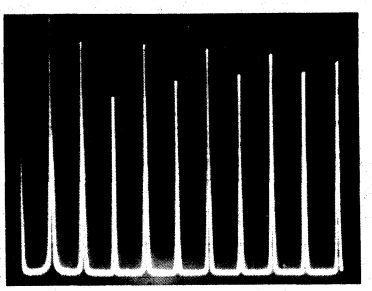
(FREQUENCY = 3.25 MHz)
BANDWIDTH = 10 kHz
SCAN WIDTH = 1 MHz/cm
CENTER FREQUENCY = 4 MHz

Figure 31– Local Oscillator Spectrum



BANDWIDTH = 10 kHz
SCAN WIDTH = 1 MHz
CENTER FREQUENCY = 4 MHz

Figure 32 – Mixer Output Spectrum



(FUNDAMENTAL 1 MHz)
BANDWIDTH = 10 kHz
SCAN WIDTH = 1 MHz/cm
CENTER FREQUENCY = 4 MHz

Figure 33 – Reference Oscillator Spectrum

occurs when the phase error is 90°. The primary disadvantage of these systems is the feed-through at twice the reference frequency. This requires a high degree of attenuation in the loop filter (at $2f_r$) to prevent frequency modulation of the voltage controlled oscillator.

On close examination it appears that a lower noise method for phase locking in a digital system could be achieved if the "edges" of the reference and feedback frequencies could be matched in time with the error voltage proportional to the time differential (phase error). For the TTL family it is easier to provide the edge matching function of the falling edges (logic 1 to logic Ø transition) of the waveform.

It is also desirable to be insensitive to the duty cycle of the two inputs. This is necessary in the proposed systems since the duty of the programmable divider changes with N. In addition, the phase detection system must be able to discriminate frequency. This is important if a tuning range of greater than two to one is used. Prior systems generally were prone to locking on harmonics of the reference frequency.

The logic required to perform this function is shown in Figure 34. This circuit contains storage for detecting a negative transition at each input, and logic for resetting the outputs if a negative transition occurs at both inputs.

To understand the operation in the system observe the waveforms of Figure 35. Notice that both outputs are initially at the 1 state. The output representing $f_1 > f_2$ is pulsed to the Ø state and reset at the rate of f_2. The minimum duty cycle of the Ø level is $(1 - f_2/f_1) \cdot 100\%$, and is cyclic at the rate of f_2.

Figure 36 shows f_1 equal to f_2 but leading in phase. The output width is equal to the time difference between the edges of f_1 and f_2. When the system is in lock, the pulse output of the phase detector is nonexistent; therefore, the filtering requirement is minimal.

At this point in the system it is necessary to make the transformation from digital to analog. This is done with the use of a "charge pump" circuit which produces plus or minus one diode drop with respect to two diode drops to ground.

The gain of the phase detector is $V/2\pi (\Phi_r - \Phi_f)$. This voltage is applied to an amplifier with a two diode dc threshold as shown in Figure 37. The amplifier also serves as an active filter whose transfer

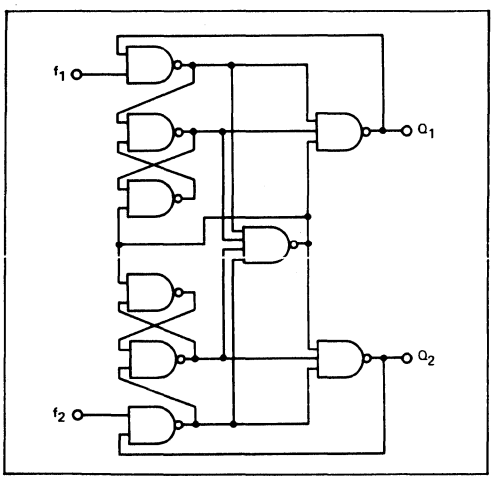


Figure 34 — Digital Phase Detector

function for $R_1 \geqslant R_2$ is: $(1 + R_2C_s)/R_1C_s$. R_1, R_2, and C determine the time constants for the loop response.

For a dynamic illustration of this operation consider the system of Figure 38. The first oscillator puts out 100 pulses at each of two different frequencies. This allows a step change in frequency to be applied to a loop so that the response to a step change can be examined. The underdamped, overdamped, and critically damped cases are shown in Figures 39, 40 and 41 respectively, with A representing the input, B the output, and C the voltage input to the oscillator.

The voltage applied to the oscillator is the superposition of the "pump up" and "pump down" pulses from the charge pump, on the dc level that controls the oscillator frequency.

When using the phase detector in the mixing system, it is important to note that the outputs are

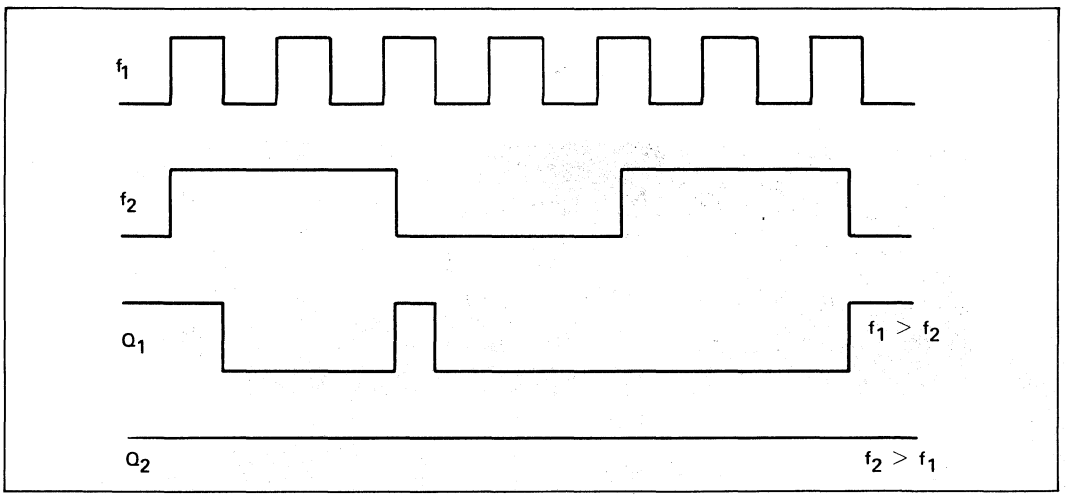


Figure 35 — Timing Diagram: Phase Detector with Different Frequency Inputs

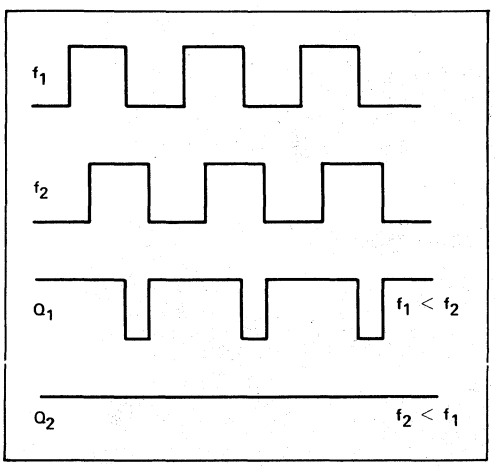


Figure 36 — Phase Detector with Equal Input Frequencies of Differing Phases

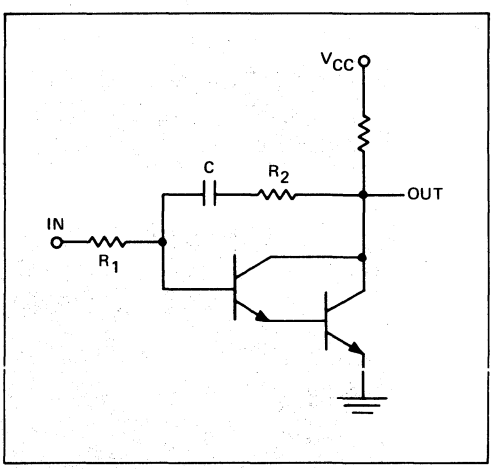


Figure 37 — Active Filter

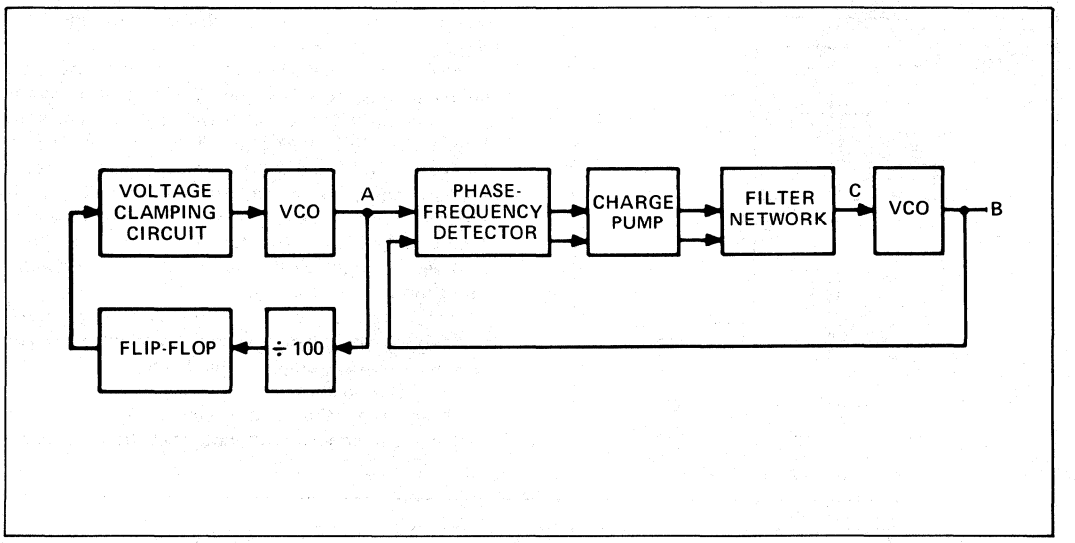


Figure 38 – System for Measuring Loop Response

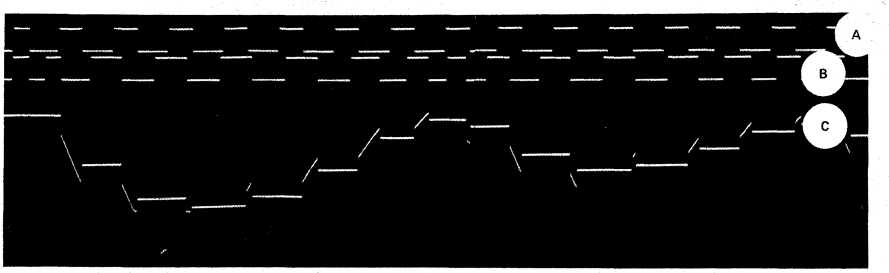


Figure 39 – Underdamped System

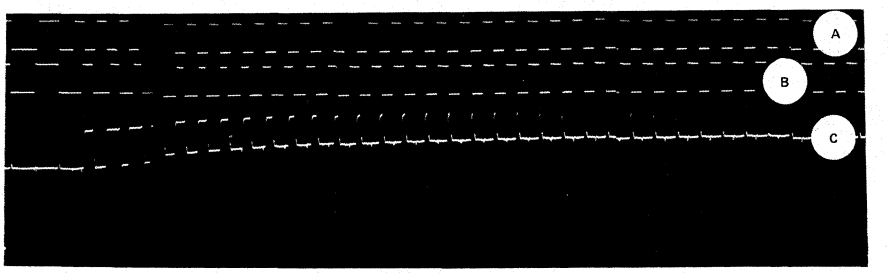


Figure 40 – Overdamped System

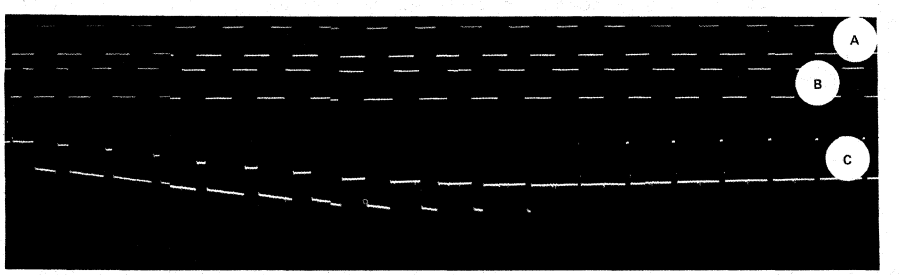
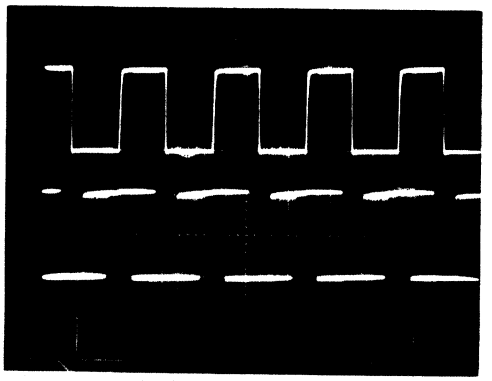
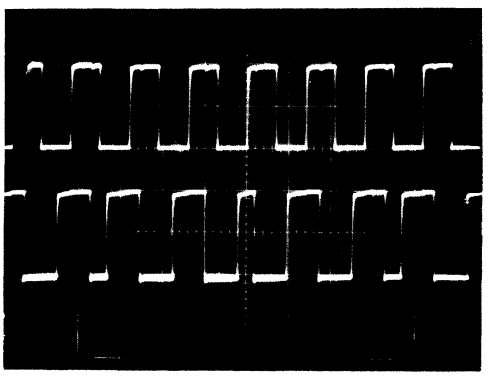


Figure 41 – Critically Damped System



TOP TRACE IS REFERENCE OSCILLATOR
BOTTOM TRACE IS MIXER OUTPUT
VERTICAL = 2V/DIV.
HORIZONTAL = 0.5 μs/DIV.

Figure 42 – Reference Oscillator and Mixer Output



TOP TRACE IS REFERENCE OSCILLATOR
BOTTOM TRACE IS MIXER OUTPUT
VERTICAL = 2V/DIV.
HORIZONTAL UNCALIBRATED

Figure 43 – Reference Oscillator and Mixer Output

always changing. It may be said that the system is never in lock, taking literally the previous definition that the error goes to zero. What the system is achieving is a stable condition based on the same number of negative transitions occurring for the feedback and for the reference (per unit time).

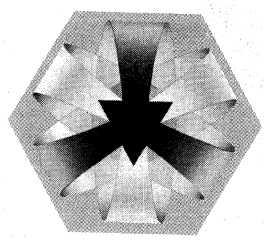
For the system shown in Figure 30, Figures 42 and 43 show the two inputs to the phase detector. The reference is purposely made continuously tunable so that a lack of coherency is achieved between the mixing frequency and the reference. In Figure 42, the oscilloscope is synchronized with the reference oscillator, and the mixer output transitions are time averaged and appear as a smear. In Figure 43 the oscilloscope is synchronized on the mixer output so that the irregularity of the waveform can be observed.

TERMINOLOGY

PLL	Phase-Locked Loop
÷	"divide by"
N	An integer
VCO	Voltage Controlled Oscillator
F (s)	A filter
ϕ	Phase detector
f_o	output frequency
VCM	Voltage Controlled Multivibrator
TTL	Transistor Transistor Logic
ECL	Emitter Coupled Logic
f_m	Mixing frequency, from a local oscillator
NBCD	Natural Binary Coded Decimal (code)
MSD	Most significant Digit
LSD	Least significant Digit
f_r	Reference Frequency

2

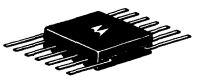
PHASE-DETECTORS



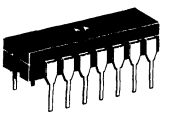
PHASE-FREQUENCY DETECTOR

MC4344 • MC4044

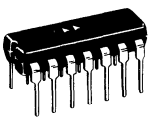
The MC4344/4044 consists of two digital phase detectors, a charge pump, and an amplifier. In combination with a voltage controlled multivibrator (such as the MC4324/4024 or MC1648), it is useful in a broad range of phase-locked loop applications. The circuit accepts MTTL waveforms at the R and V inputs and generates an error voltage that is proportional to the frequency and/or phase difference of the input signals. Phase detector #1 is intended for use in systems requiring zero frequency and phase difference at lock. Phase detector #2 is used if quadrature lock is desired. Phase detector #2 can also be used to indicate that the main loop, utilizing phase detector #1, is out of lock.



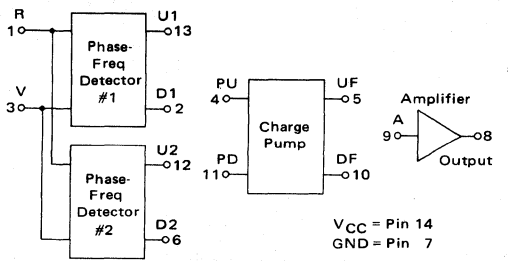
F SUFFIX
CERAMIC PACKAGE
CASE 607



L SUFFIX
CERAMIC PACKAGE
CASE 632
(TO-116)

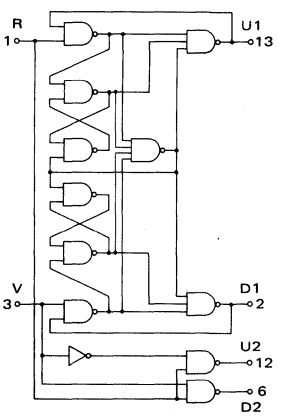


P SUFFIX
PLASTIC PACKAGE
CASE 646
MC4044 only

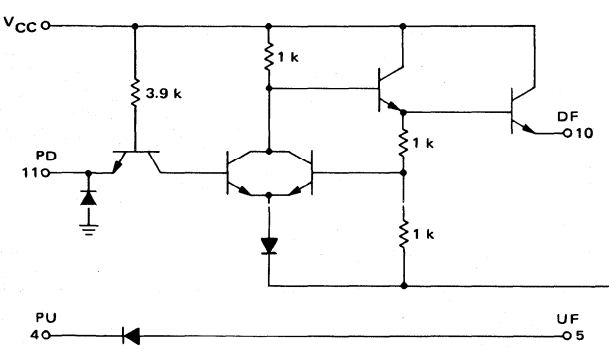


Input Loading Factor: R, V = 3
Output Loading Factor (Pin 8) = 10
Total Power Dissipation = 85 mW typ/pkg
Propagation Delay Time = 9.0 ns typ
(thru phase detector)

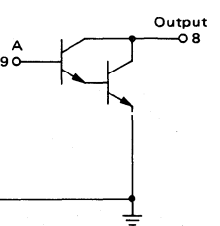
PHASE DETECTOR



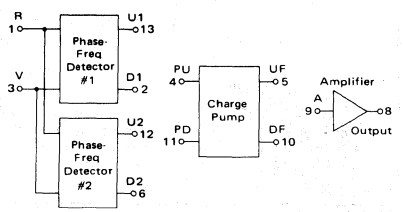
CHARGE PUMP



AMPLIFIER



ELECTRICAL CHARACTERISTICS



INPUT STATE	INPUT RI	INPUT VI	OUTPUT U1	OUTPUT D1	OUTPUT U2	OUTPUT D2
1	0	0	X	X	1	1
2	1	0	X	X	0	1
3	1	1	X	X	1	0
4	1	0	X	X	0	1
5	0	0	X	X	1	1
6	1	0	X	X	0	1
7	0	0	X	X	1	1
8	1	0	X	X	0	1
9	0	0	0	1	1	1
10	0	1	0	1	1	1
11	0	0	1	1	1	1
12	0	1	1	1	1	1
13	0	0	1	0	1	1
14	0	1	1	0	1	1
15	0	0	1	0	1	1
16	1	0	1	0	0	1
17	0	0	1	1	1	1

TRUTH TABLE

This is not strictly a functional truth table; i.e., it does not show all possible modes of operation. It is useful for dc testing.

1. X indicates output state unknown.
2. U1 and D1 outputs are sequential; i.e., they must be sequenced in order shown.
3. U2 and D2 outputs are combinational; i.e., they need only inputs shown to obtain outputs.

	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES mA I_{OL}	I_{OH1}	I_{OH2}	I_{in}	I_{IC}	I_A	Volts V_{IL}	V_{IH}	V_{IHH}	V_{ILT}	V_{IHT}	V_{out}	V_{CC}	V_{CCL}	V_{CCH}
MC4344	-55°C	20	-1.6	-1.0	–	–	0.002	0.4	2.4	–	1.1	2.0	1.5	5.0	4.5	5.5
	+25°C	20	-1.6	-1.0	1.0	-10	0.002	0.4	2.4	5.5	1.1	1.8	1.5	5.0	4.5	5.5
	+125°C	20	-1.6	-1.0	–	–	0.002	0.4	2.4	–	0.9	1.8	1.5	5.0	4.5	5.5
MC4044	0°C	20	-1.6	-1.0	–	–	0.002	0.4	2.5	–	1.1	2.0	1.5	5.0	4.75	5.25
	+25°C	20	-1.6	-1.0	1.0	-10	0.002	0.4	2.5	5.5	1.1	1.8	1.5	5.0	4.75	5.25
	+75°C	20	-1.6	-1.0	–	–	0.002	0.4	2.5	–	0.9	1.8	1.5	5.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC4344 Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC4044 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH1}	I_{OH2}	I_{in}	I_{IC}	I_A	V_{IL}	V_{IH}	V_{IHH}	V_{ILT}	V_{IHT}	V_{out}	V_{CC}	V_{CCL}	V_{CCH}	Pulse 1	Gnd
Input																																
Forward Current	I_{IL}	1	–	-4.8	–	-4.8	–	-4.8	–	-4.8	–	-4.8	–	-4.8	mAdc	–	–	–	–	–	–	1	–	–	–	–	–	–	–	14	–	7
		3	–	-4.8	–	-4.8	–	-4.8	–	-4.8	–	-4.8	–	-4.8		–	–	–	–	–	–	3	–	–	–	–	–	–	–	↓	–	↓
		11	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6		–	–	–	–	–	–	11	–	–	–	–	–	–	–		–	
Leakage Current	I_{IH}	1	–	120	–	120	–	120	–	120	–	120	–	120	μAdc	–	–	–	–	–	–	–	1	–	–	–	–	–	–	14	–	7
		3	–	120	–	120	–	120	–	120	–	120	–	120		–	–	–	–	–	–	–	3	–	–	–	–	–	–	14	–	7
		4	–	5.0	–	5.0	–	5.0	–	5.0	–	5.0	–	5.0		–	–	–	–	–	–	–	–	–	–	–	–	–	–	4	–	5,7
		11	–	40	–	40	–	40	–	40	–	40	–	40	↓	–	–	–	–	–	–	–	11	–	–	–	–	–	–	14	–	7
	I_{IHH}	1	–	–	1.0	–	–	–	–	–	1.0	–	–	–	mAdc	–	–	–	–	–	–	–	–	1	–	–	–	–	–	14	–	7
		3	–	–	↓	–	–	–	–	–	↓	–	–	–		–	–	–	–	–	–	–	–	3	–	–	–	–	–	↓	–	↓
		11	–	–		–	–	–	–	–		–	–	–		–	–	–	–	–	–	–	–	11	–	–	–	–	–		–	
Clamp Voltage	V_{IC}	1	–	–	–	-1.5	–	–	–	–	–	-1.5	–	–	Vdc	–	–	–	–	–	1	–	–	–	–	–	–	–	14	–	–	7
		3	–	–	–	-1.5	–	–	–	–	–	-1.5	–	–	Vdc	–	–	–	–	–	3	–	–	–	–	–	–	–	14	–	–	7
Output (Note 1)																																
Output Voltage	V_{OH}	6	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	6	–	–	–	–	–	–	–	1,3	–	–	–	14	–	–	7
		12	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	12	–	–	–	–	–	–	–	1,3	–	–	–	14	–	–	7
	**		–	–	–	–	–	–	–	–	–	–	–	–		–	–	–	–	–	–	–	–	–	3	1	–	–	14	–	–	7
	V_{OL}	6	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	6	–	–	–	–	–	–	–	–	–	1,3	–	–	14	–	–	7
	V_{OH}	12	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	12	–	–	–	–	–	–	–	–	1,3	–	–	14	–	–	7
	**		–	–	–	–	–	–	–	–	–	–	–	–	Vdc	–	–	–	–	–	–	–	–	–	3	1	–	–	14	–	–	7
	**		–	–	–	–	–	–	–	–	–	–	–	–	Vdc	–	–	–	–	–	–	–	–	–	1,3	–	–	–	14	–	–	7
	V_{OH}	6	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	6	–	–	–	–	–	–	–	3	1	–	–	14	–	–	7
	V_{OL}	12	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	12	–	–	–	–	–	–	–	–	3	1	–	–	14	–	–	7
	**		–	–	–	–	–	–	–	–	–	–	–	–	Vdc	–	–	–	–	–	–	–	–	–	1,3	–	–	–	14	–	–	7
	**		–	–	–	–	–	–	–	–	–	–	–	–	Vdc	–	–	–	–	–	–	–	–	–	3	1	–	–	14	–	–	7
	V_{OH}	2	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	2	–	–	–	–	–	–	–	1,3	–	–	–	14	–	–	7
	V_{OL}	13	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	13	–	–	–	–	–	–	–	–	1,3	–	–	–	14	–	–	7
	V_{OH}	2	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	2	–	–	–	–	–	–	–	1	3	–	–	14	–	–	7
	V_{OL}	13	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	13	–	–	–	–	–	–	–	–	1	3	–	–	14	–	–	7
	V_{OH}	2	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	2	–	–	–	–	–	–	–	1,3	–	–	–	14	–	–	7
		13	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	13	–	–	–	–	–	–	–	1,3	–	–	–	14	–	–	7
	V_{OL}	2	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	2	–	–	–	–	–	–	–	–	1,3	–	–	–	14	–	–	7
	V_{OH}	13	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	13	–	–	–	–	–	–	–	1,3	–	–	–	14	–	–	7
	V_{OL}	2	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	2	–	–	–	–	–	–	–	–	1	3	–	–	14	–	–	7
	V_{OH}	13	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	13	–	–	–	–	–	–	–	1	3	–	–	14	–	–	7
	V_{OL}	2	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	2	–	–	–	–	–	–	–	–	1,3	–	–	–	14	–	–	7
	V_{OH}	13	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	13	–	–	–	–	–	–	–	1,3	–	–	–	14	–	–	7
	V_{OL}	2	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	2	–	–	–	–	–	–	–	–	3	1	–	–	14	–	–	7
	V_{OH}	13	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	13	–	–	–	–	–	–	–	3	1	–	–	14	–	–	7
	V_{OH}	2	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	2	–	–	–	–	–	–	–	1,3	–	–	–	14	–	–	7
		13	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	13	–	–	–	–	–	–	–	1,3	–	–	–	14	–	–	7
Short-Circuit Current	I_{OS}	2	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	mAdc	–	–	–	–	–	–	–	–	–	–	1	–	–	–	14	2,3,7
		6	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓		–	–	–	–	–	–	–	–	–	–	–	–	–	14	–	–	1,3,6,7
		12														–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	1,3,7,12
		13														–	–	–	–	–	–	–	–	–	–	–	–	–	–	1	–	3,7,13
Leakage Current	I_{OLK}	2	–	250	–	250	–	250	–	250	–	250	–	250	μAdc	–	–	–	–	–	–	–	–	–	–	1	–	2,14	–	–	–	3,7
		6	–	↓	–	↓	–	↓	–	↓	–	↓	–	↓		–	–	–	–	–	–	–	–	–	–	–	–	6,14	–	–	–	1,3,7
		12	–		–		–		–		–		–			–	–	–	–	–	–	–	–	–	–	–	–	12,14	–	–	–	1,3,7
		13	–		–		–		–		–		–			–	–	–	–	–	–	–	–	–	–	1	–	13,14	–	–	–	3,7
Collector-Emitter Voltage	V_{CE}	5	–	–	0.5	–	–	–	–	–	0.5	–	–	–	Vdc	–	–	–	5	–	–	–	–	–	–	–	–	–	–	–	–	4,7
Output Voltage	V_{EH}	10	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	Vdc	–	–	10	–	–	–	–	–	–	11	–	–	–	14	–	–	7
Output Current	I_O	8	0.2	–	0.8	–	1.0	–	0.5	–	0.8	–	1.0	–	mAdc	–	–	–	–	–	9	–	–	–	–	–	–	–	8	–	–	7
Leakage Current	I_{OLK}	8	–	120	–	120	–	120	–	120	–	120	–	120	μAdc	–	–	–	–	–	–	–	–	–	–	–	–	–	8	–	7,9	
		10	–	5.0	–	5.0	–	5.0	–	5.0	–	5.0	–	5.0	μAdc	–	–	–	–	–	–	–	11	–	–	–	10	–	14	–	7	
Power Requirements (Total Device)																																
Power Supply Drain	I_{CC}	14	–	40	–	40	–	40	–	40	–	40	–	40	mAdc	–	–	–	–	–	–	–	–	–	–	–	–	14	–	–	–	7

Note 1. The outputs of the device must be tested by sequencing through the indicated input states according to the truth table and functional diagram. All input, power supply and ground voltages must be maintained between tests unless otherwise noted. Procedures identified by a double asterisk (**) in the Symbol column are necessary to change the state of the sequential logic.

Pulse 1: V_{CCL} ⌐ V_{CC} Used to change power supply voltage from previous test.

MAXIMUM RATINGS

Rating		Value	Unit
Supply Operating Voltage Range	MC4344 MC4044	4.5 to 5.5 4.75 to 5.25	Vdc
Supply Voltage		+7.0	Vdc
Input Voltage		+5.5	Vdc
Output Voltage		+5.5	Vdc
Operating Temperature Range	MC4344 MC4044	-55 to +125 0 to +75	°C
Storage Temperature Range – Ceramic Package Plastic Package		-65 to +150 -55 to +125	°C
Maximum Junction Temperature	MC4344 MC4044	+175 +150	°C
Thermal Resistance - Junction To Case (θ_{JC}) Flat Ceramic Package Dual In-Line Ceramic Package Plastic Package		 0.06 0.05 0.07	°C/mW
Thermal Resistance - Junction To Ambient (θ_{JA}) Flat Ceramic Package Dual In-Line Ceramic Package Plastic Package		 0.21 0.15 0.15	°C/mW

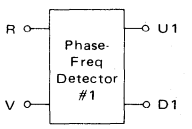
CONTENTS

OPERATING CHARACTERISTICS

Operation of the MC4344/4044 is best explained by initially considering each section separately. If phase detector #1 is used, loop lockup occurs when both outputs U1 and D1 remain high. This occurs only when all the negative transitions on R, the reference input, and V, the variable or feedback input, coincide. The circuit responds only to transitions, hence phase error is independent of input waveform duty cycle or amplitude variation. Phase detector #1 consists of sequential logic circuitry, therefore operation prior to lockup is determined by initial conditions.

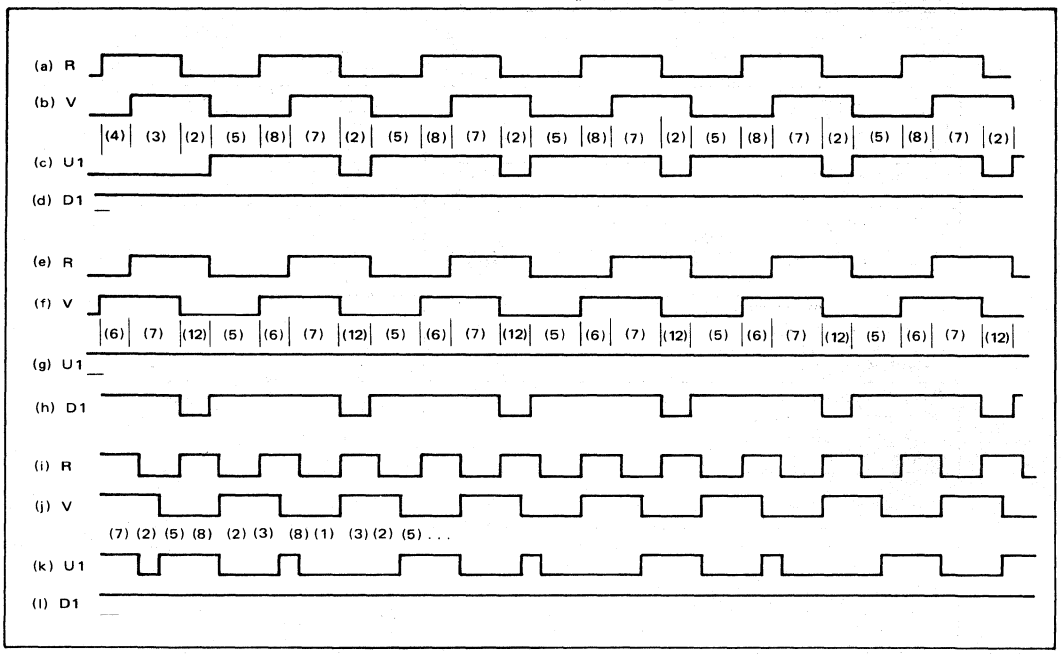
When operation is initiated, by either applying power to the circuit or active input signals to R and V, the circuitry can be in one of several states. Given any particular starting conditions, the flow table of Figure 1 can be used to determine subsequent operation. The flow table indicates the status of U1 and D1 as the R and V inputs are varied. The numbers in the table which are in parentheses are arbitrarily assigned labels that correspond to stable states that can result for each input combination. The numbers without parentheses refer to unstable conditions. Input changes are traced by horizontal movement in the table; after each input change, circuit operation will settle in the numbered state indicated by moving horizontally to the appropriate R-V column. If the number at that

FIGURE 1 – PHASE DETECTOR #1 FLOW TABLE



R-V 0-0	R-V 0-1	R-V 1-1	R-V 1-0	U1	D1
(1)	2	3	(4)	0	1
5	(2)	(3)	8	0	1
(5)	6	7	8	1	1
9	(6)	7	12	1	1
5	2	(7)	12	1	1
1	2	7	(8)	1	1
(9)	(10)	11	12	1	0
5	6	(11)	(12)	1	0

FIGURE 2 – PHASE DETECTOR #1 TIMING DIAGRAM



location is not in parentheses, move vertically to the number of the same value that is in parentheses. For a given input pair, any one of three stable states can exist. As an example, if R = 1 and V = 0, the circuit will be in one of the stable states (4), (8), or (12).

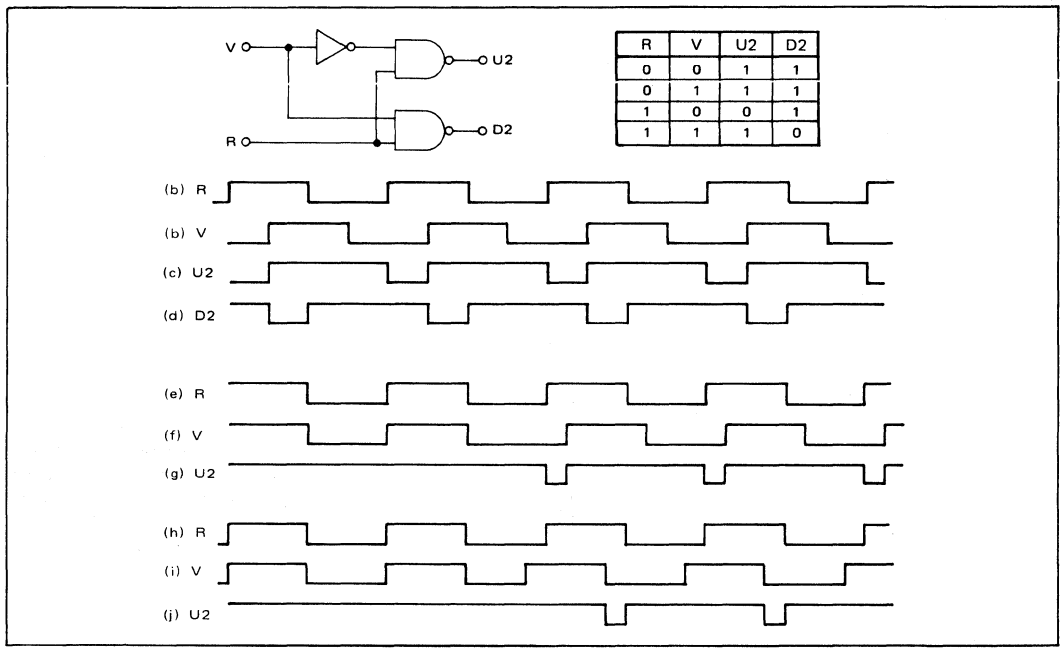
Use of the table in determining circuit operation is illustrated in Figure 2. In the timing diagram, the input to R is the reference frequency; the input to V is the same frequency but lags in phase. Stable state (4) is arbitrarily assumed as the initial condition. From the timing diagram and flow table, when the circuit is in stable state (4), outputs U1 and D1 are "0" and "1" respectively. The next input state is R-V = 1-1; moving horizontally from stable state (4) under R-V = 1-0 to the R-V = 1-1 column, state 3 is indicated. However, this is an unstable condition and the circuit will assume the state indicated by moving vertically in the R-V = 1-1 column to stable state (3). In this instance, outputs U1 and D1 remain unchanged. The input states next become R-V = 0-1; moving horizontally to the R-V = 0-1 column, stable state (2) is indicated. At this point there is still no change in U1 or D1. The next input change shifts operation to the R-V = 0-0 column where unstable state 5 is indicated. Moving vertically to stable state (5), the outputs now change state to U1-D1 = 1-1. The next input change, R-V = 1-0, drives the circuitry to stable state (8), with no change in U1 or D1. The next input, R-V = 1-1, leads to stable state (7) with no change in the outputs. The next two input state changes cause U1 to go low between the negative transitions of R and V. As the inputs continue to change, the circuitry moves repeatedly through stable states (2), (5), (8), (7), (2), etc. as shown, and a periodic waveform is obtained on the U1 terminal while D1 remains high.

A similar result is obtained if V is leading with respect to R, except that the periodic waveform now appears on D1 as shown in rows e-h of the timing diagram of Figure 2. In each case, the average value of the resulting waveform is proportional to the phase difference between the two inputs. In a closed loop application, the error signal for controlling the VCO is derived by translating and filtering these waveforms.

The results obtained when R and V are separated by a fixed frequency difference are indicated in rows i-l of the timing system. For this case, the U1 output goes low when R goes low and stays in that state until a negative transition on V occurs. The resulting waveform is similar to the fixed phase difference case, but now the duty cycle of the U1 waveform varies at a rate proportional to the difference frequency of the two inputs, R and V. It is this characteristic that permits the MC4344/4044 to be used as a frequency discriminator; if the signal on R has been frequency modulated and if the loop bandwidth is selected to pass the deviation frequency but reject R and V, the resulting error voltage applied to the VCO will be the recovered modulation signal.

Phase detector #2 consists only of combinatorial logic, therefore its characteristics can be determined from the

FIGURE 3 – PHASE DETECTOR #2 OPERATION



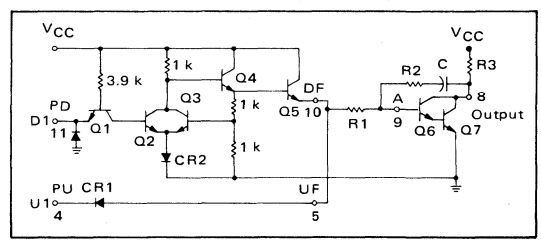
R	V	U2	D2
0	0	1	1
0	1	1	1
1	0	0	1
1	1	1	0

simple truth table of Figure 3. Since circuit operation requires that both inputs to the charge pump either be high or have the same duty cycle when lock occurs, using this phase detector leads to a quadrature relationship between R and V. This is illustrated in rows a-d of the timing diagram of Figure 3. Note that any deviation from a fifty percent duty cycle on the inputs would appear as phase error.

Waveforms showing the operation of phase detector #2 when phase detector #1 is being used in a closed loop are indicated in rows e-j. When the main loop is locked, U2 remains high. If the loop drifts out of lock in either direction a negative pulse whose width is proportional to the amount of drift appears on U2. This can be used to generate a simple loss-of-lock indicator.

Operation of the charge pump is best explained by considering it in conjunction with the Darlington amplifier included in the package (see Figure 4). There will be a pulsed waveform on either PD or PU, depending on the phase-frequency relationship of R and V. The charge pump serves to invert one of the input waveforms (D1) and translates the voltage levels before they are applied to the loop filter. When PD is low and PU is high, Q1 will be conducting in the normal direction and Q2 will be off. Current will be flowing through Q3 and CR2; the base of Q3 will be two V_{BE} drops above ground or approximately 1.5 volts. Since both of the resistors connected to the base of Q3 are equal, the emitter of Q4 (base of Q5) will be

FIGURE 4 – CHARGE PUMP OPERATION



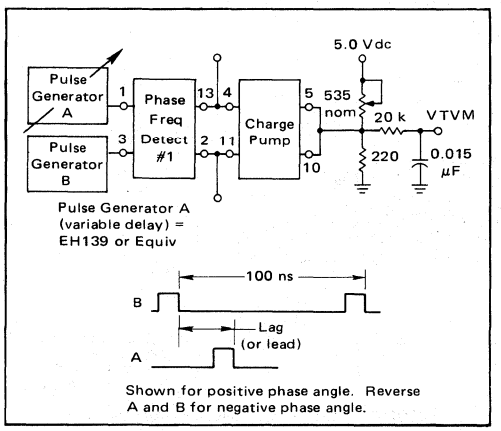
approximately 3.0 volts. For this condition, the emitter of Q5 (DF) will be one V_{BE} below this voltage, or about 2.25 volts. The PU input to the charge pump is high (> 2.4 volts) and CR1 will be reverse biased. Therefore Q5 will be supplying current to Q6. This will tend to lower the voltage at the collector of Q7, resulting in an error signal that lowers the VCO frequency as required by a "pump down" signal.

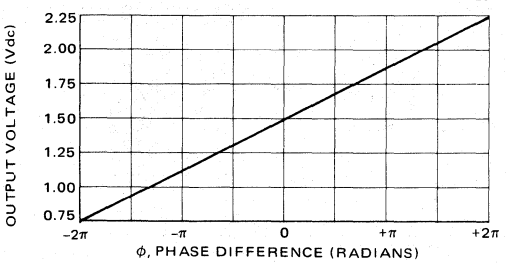
When PU is low and PD is high, CR1 is forward biased and UF will be approximately one V_{BE} above ground (neglecting the $V_{CE(sat)}$ of the driving gate). With PD high, Q1 conducts in the reverse direction, supplying base current for Q2. While Q2 is conducting, Q4 is prevented from supplying base drive to Q5; with Q5 cut off and UF low there is no base current for Q6 and the voltage at the

collector of Q7 moves up, resulting in an increase in the VCO operating frequency as required by a "pump up" signal.

If both inputs to the charge pump are high (zero phase difference), both CR1 and the base-emitter junction of Q5 are reverse biased and there is no tendency for the error voltage to change. The output of the charge pump varies between one V_{BE} and three V_{BE} as the phase difference of R and V varies from minus 2π to plus 2π. If this signal is filtered to remove the high-frequency components, the phase detector transfer function, K_ϕ, of approximately 0.12 volt/radian is obtained (see Figure 5).

FIGURE 5 – PHASE DETECTOR TEST





The specified gain constant of 0.12 volt/radian may not be obtained if the amplifier/filter combination is improperly designed. As indicated previously, the charge pump delivers pump commands of about 2.25 volts on the positive swings and 0.75 volt on the negative swings for a mean no-pump value of 1.5 volts. If the filter amplifier is biased to threshold "on" at 1.5 volts, then the pump up and down voltages have equal effects. The pump signals are established by V_{BE}'s of transistors with milliamperes of current flowing. On the other hand, the transistors included for use as a filter amplifier will have very small currents flowing and will have correspondingly lower V_{BE}'s – on the order of 0.6 volt each for a threshold of 1.2 volts. Any displacement of the threshold from 1.5 volts causes an increase in gain in one direction and a reduction in the other. The transistor configuration provided is hence not optimum but does allow for the use of an additional transistor to improve filter response. This addition also results in a non-symmetrical response since the threshold is now approximately 1.8 volts. The effective positive swing is limited to 0.45 volt while the negative swing below threshold can be greater than 1.0 volt. This means that the loop gain when changing from a high frequency to a lower frequency is less than when changing in the opposite direction. For type two loops this tends to increase overshoot when going from low to high and increases damping in the other direction. These problems and the selection of external filter components are intimately related to system requirements and are discussed in detail in the filter design section.

PHASE-LOCKED LOOP COMPONENTS

General

A basic phase-locked loop, when operating properly, will acquire ("lock on") an input signal, track it in frequency, and exhibit a fixed phase relationship relative to the input. In this basic loop, the output frequency will be identical to the input frequency (Figure 6). A fundamental loop consists of a phase detector, amplifier/filter, and voltage-controlled oscillator (Figure 7). It appears and acts like a unity gain feedback loop. The controlled variable is phase; any error between f_{in} and f_{out} is amplified and applied to the VCO in a corrective direction.

FIGURE 6 – BASIC PHASE-LOCKED LOOP FREQUENCY RELATIONSHIP

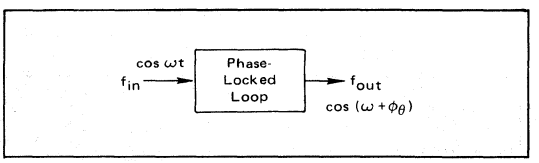
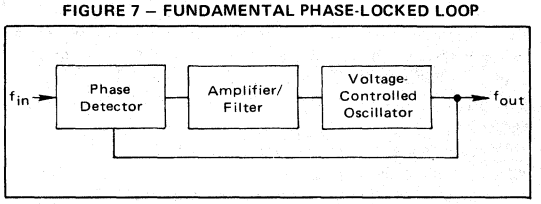


FIGURE 7 – FUNDAMENTAL PHASE-LOCKED LOOP



Simple phase detectors in digital phase-locked loops usually put out a series of pulses. The average value of these pulses is the "gain constant", K_ϕ, of the phase detector – the volts out for a given phase difference, expressed as volts/radian.

The VCO is designed so that its output frequency range is equal to or greater than the required output frequency range of the system. The ratio of change in output frequency to input control voltage is called "gain constant", K_O. If the slope of f_{out} to V_{in} is not linear (i.e., changes greater than 25%) over the expected frequency range, the

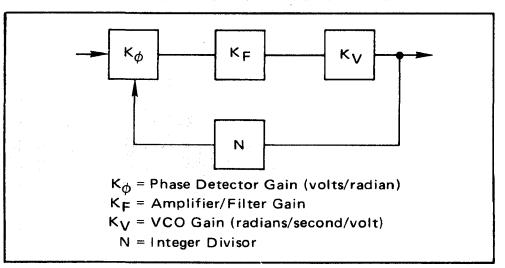
curve should be piece-wise approximated and the appropriate constant applied for "best" and "worst" case analysis of loop performance.

System dynamics when in lock are determined by the amplifier/filter block. Its gain determines how much phase error exists between f_{in} and f_{out}, and filter characteristics shape the capture range and transient performance. This will be discussed in detail later.

Loop Filter

Fundamental loop characteristics such as capture range, loop bandwidth, capture time, and transient response are controlled primarily by the loop filter. The loop behavior is described by gains in each component block of Figure 8.

FIGURE 8 – GAIN CONSTANTS



The output to input ratio reflects a second order low pass filter in frequency response with a static gain of N:

$$\frac{\theta_O(s)}{\theta_i(s)} = \frac{K_\phi K_F K_V}{s + \frac{K_\phi K_F K_V}{N}} \quad (1)$$

where: $$K_F = \frac{1 + T_1 s}{T_2 s} \quad (2)$$

$T_1 = R_2C$ and $T_2 = R_1C$ of Figure 4. Therefore,

$$\frac{\theta_O(s)}{\theta_i(s)} = \frac{N(1 + T_1 s)}{\frac{s^2 N T_2}{K_\phi K_V} + T_1 s + 1} \quad (3)$$

Both ω_n (loop bandwidth or natural frequency) and ζ (damping factor) are particularly important in the transient response to a step input of phase or frequency (Figure 9), and are defined as:

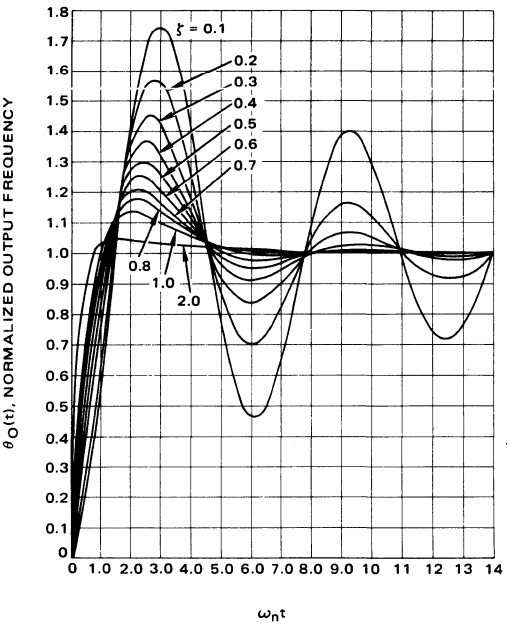
$$\omega_n = \sqrt{\frac{K_\phi K_V}{NT_2}} \quad (4)$$

$$\zeta = \sqrt{\frac{K_\phi K_V}{NT_2}} \left(\frac{T_1}{2}\right) \quad (5)$$

Using these terms in Equation 3,

$$\frac{\theta_O(s)}{\theta_i(s)} = \frac{N(1 + T_1 s)}{\frac{s^2}{\omega_n^2} + \frac{2\zeta s}{\omega_n} + 1} \quad (6)$$

FIGURE 9 – TYPE 2 SECOND ORDER STEP RESPONSE



In a well defined system controlling factors such as ω_n and ζ may be chosen either from a transient basis (time domain response) or steady state frequency plot (roll-off point and peaking versus frequency). Once these two design goals are defined, synthesis of the filter is relatively straight-forward.

Constants K_ϕ, K_V, and N are usually fixed due to other design constraints, leaving T_1 and T_2 as variables to set ω_n and ζ. Since only T_2 appears in Equation 4, it is the easiest to solve for initially.

$$T_2 = \frac{K_\phi K_V}{N\omega_n^2} \quad (7)$$

From Equation 5, we find

$$T_1 = \frac{2\zeta}{\omega_n} \quad (8)$$

Using relationships 7 and 8, actual resistor values may be computed:

$$R_1 = \frac{K_\phi K_V}{N\omega_n^2 C} \quad (9)$$

$$R_2 = \frac{2}{\omega_n C} \quad (10)$$

Although fundamentally the range of R_1 and R_2 may be from several hundred to several thousand ohms, sideband considerations usually force the value of R_1 to be set first, and then R_2 and C computed.

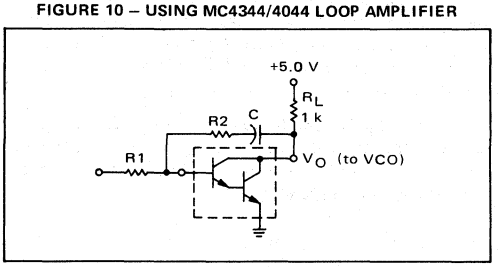
$$C = \frac{K_\phi K_V}{N\omega_n^2 R_1} \quad (11)$$

Calculation of passive components R_2 and C (in synthesizers) is complicated by incomplete information on N, which is variable, and the limits of ω_n and ζ during that variance. Equally important are changes in K_V over the output frequency range. Minimum and maximum values of ω_n and ζ can be computed from Equations 4 and 5 when the appropriate worst case numbers are known for all the factors.

Amplifier/filter gain usually determines how much phase error exists between f_{in} and f_{out}, and the filter characteristic shapes capture range and transient performance. A relatively simple, low gain amplifier may usually be used in the loop since many designs are not constrained so much by phase error as by the need to make f_{in} equal f_{out}. Unnecessarily high gains can cause problems in linear loops when the system is out of lock if the amplifier output swing is not adequately restricted since integrating operational amplifier circuits will latch up in time and effectively open the loop.

The internal amplifier included in the MC4344/4044 may be used effectively if its limits are observed. The circuit configuration shown in Figure 10 illustrates the

FIGURE 10 – USING MC4344/4044 LOOP AMPLIFIER



placement of R_1, R_2, C, and load resistor R_L (1 kΩ). Due to the non-infinite gain of this stage ($A_V \approx 30$) and other non-ideal characteristics, some restraint must be placed on passive component selection. Foremost is a lower limit on the value of R_2 and an upper limit on R_1. Placed in order of priority, the recommendations are as follows: (a) $R2 > 50\ \Omega$, (b) $R2/R1 \leq 10$, (c) $1\ k\Omega < R1 < 5\ k\Omega$.

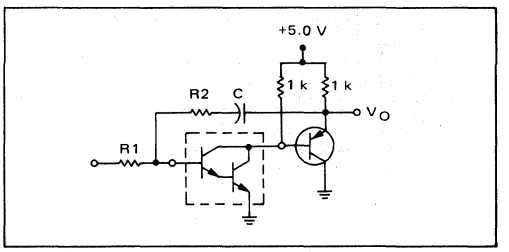
Limit (c) is the most flexible and may be violated with either higher sidebands and phase error ($R_1 > 5\ k\Omega$) or lower phase detector gain ($R_1 < 1\ k\Omega$). If limit (b) is exceeded, loop bandwidth will be less than computed and may not have any similarity to the prediction. For an accurate reproduction of calculated loop characteristics one should go to an operational amplifier which has sufficient gain to make limit (b) readily satisfied. Limit (a) is very important because T_1 in Equation 5 is in reality composed of three elements:

$$T_1 = C\left(R_2 - \frac{1}{g_m}\right) \quad (12)$$

where g_m = transconductance of the common emitter amplifier.

Normally g_m is large and T_1 nearly equals R_2C, but resistance values below 50 Ω can force the phase-compensating "zero" to infinity or worse (into the right half plane) and give an unstable system. The problem can be circumvented to a large degree by buffering the feedback with an emitter follower (Figure 11). Inequality (a) may

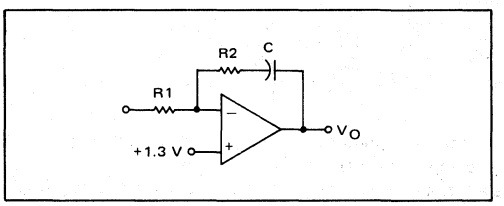
FIGURE 11 – AMPLIFIER CAPABLE OF HANDLING LOWER R2



then be reduced by at least an order of magnitude ($R_2 > 5\ \Omega$) keeping in mind that electrolytic capacitors used as C may approach this value by themselves at the frequency of interest (ω_n).

Larger values of R_1 may be accommodated by either using an operational amplifier with a low bias current ($I_b < 1.0\ \mu A$) as shown in Figure 12 or by buffering the internal

FIGURE 12 – USING AN OPERATIONAL AMPLIFIER TO EXTEND THE VALUE OF R1



Darlington pair with an FET (Figure 13). It is vitally important, however, that the added device be operated at zero V_{GS}. Source resistor R_4 should be adjusted for this condition (which amounts to I_{DSS} current for the FET). This insures that the overall amplifier input threshold remains at the proper potential of approximately two base-emitter drops. Use of an additional emitter follower instead of the FET and R_4 (Figure 14) gives a threshold near the upper limit of the phase detector charge pump, resulting in an extremely unsymmetrical phase detector gain in the pump up versus pump down mode. It is not unusual to

FIGURE 13 – FET BUFFERING TO RAISE AMPLIFIER INPUT IMPEDANCE

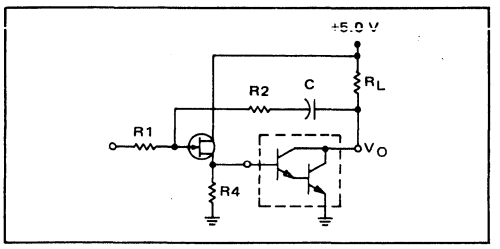
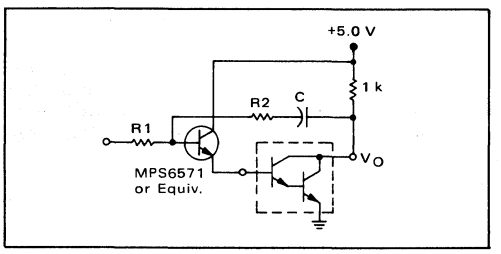


FIGURE 14 – EMITTER FOLLOWER BUFFERING OF AMPLIFIER INPUT



note a 5:1 difference in K_ϕ for circuits having the bipolar buffer stage. If the initial design can withstand this variation in loop gain and remain stable, the approach should be considered since there are no critical adjustments as in the FET circuit.

DESIGN PROBLEMS AND THEIR SOLUTIONS

Dynamic Range

A source of trouble for all phase-locked loops, as well as most electronics is simply overload or lack of sufficient dynamic range. One limit is the amplifier output drive to the VCO. Not only must a designer note the outside limits of the dc control voltage necessary to give the output frequency range, he must also account for the worst case of overshoot expected for the system. Relatively large damping factors (ζ = 0.5) can contribute significant amounts of overshoot (30%). To be prepared for the worst case output swing the amplifier should have as much margin to positive and negative limits as the expected swing itself. That is, if a two-volt swing is sufficient to give the desired output frequency excursion, there should be at least a two-volt cushion above and below maximum expected steady-state values on the control line.

This increase in range, in order to be effective, must of course be followed by an equivalent range in the VCO or there is little to be gained. Any loss in loop gain will in general cause a decrease in ζ and a consequent increase in overshoot and ringing. If the loss in gain is caused by saturation or near saturation conditions, the problem tends to accelerate towards a situation where the system settles in not only a slow but oscillatory manner as well.

Loss of amplifier gain may not be due entirely to normal system damping considerations. In loops employing digital phase detectors, an additional problem is likely to appear. This is due to amplifier saturation during a step input when there is a maximum phase detector output simultaneous with a large transient overshoot. The phase detector square wave rides on top of the normal transient and may even exceed the amplifier output limits imposed above. Since the input frequency will exceed the R_2C time constant, gain K_F for these annoying pulses will be R_2/R_1. Ordinarily this ratio will be less than 1, but some circumstances dictate a low loop gain commensurate with a fairly high ω_n. For these cases, R_2/R_1 may be higher than 10 and cause pulse-wise saturation of the amplifier. Since the dc control voltage is an average of phase detector pulses, clipping can be translated into a reduction in gain with all the "benefits" already outlined, i.e., poor settling time. An easy remedy to apply in many cases is a simple RC low pass section preceding or together with the integrator-lag section. To make transient suppression independent of amplifier response, the network may be imbedded within the input resistor R_1 (Figure 15) or be implemented

FIGURE 15 – IMPROVED TRANSIENT SUPPRESSION WITH R1 – C_c

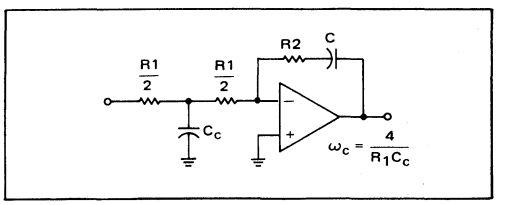
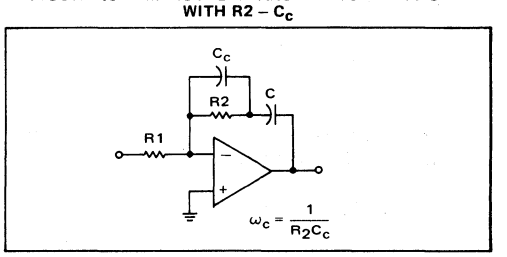


FIGURE 16 – IMPROVED TRANSIENT SUPPRESSION WITH R2 – C_c



by placing a feedback capacitor across R_2 (Figure 16). Besides rounding off and inhibiting pulses, these networks add an additional pole to the loop and may cause further overshoot if the cutoff frequency (ω_c) is too close to ω_n. If at all possible the cutoff point should be five to ten times ω_n. How far ω_c can be placed from ω_n depends on the input frequency relationship to ω_n since f_{in} is, after all, what is being filtered. A side benefit of this simple RC pulse "flattener" is a reduction in f_{in} sidebands around f_{out} for synthesizers with N > 1. However, a series of RC filters is not recommended for either extended

pulse suppression or sideband improvement as excess phase will begin to build up at the loop crossover ($\approx \omega_n$) and tend to cause instability. This will be discussed in more detail later.

Spurious Outputs

Although the major problem in phase-locked loop design is defining loop gain and phase margin under dynamic operating conditions, high-quality synthesizer designs also require special consideration to minimize spurious spectral components – the worst of which is reference-frequency sidebands. Requirements for good sideband suppression often conflict with other performance goals – loop dynamic behavior, suppression of VCO noise, or suppression of other in-loop noise. As a result, most synthesizer designs require compromised specifications. For a given set of components and loop dynamic conditions, reference sidebands should be predicted and checked against design specifications before any hardware is built.

Any steady-state signal on the VCO control will produce sidebands in accordance with normal FM theory. For small spurious deviations on the VCO, relative sideband-to-carrier levels can be predicted by:

$$\frac{\text{sidebands}}{\text{carrier}} \cong \frac{V_{ref} K_V}{2\omega_{ref}} \qquad (13)$$

where V_{ref} = peak voltage value of spurious freuqency at the VCO input.

Unwanted control line modulation can come from a variety of sources, but the most likely cause is phase detector pulse components feeding through the loop filter. Although the filter does establish loop dynamic conditions, it leaves something to be desired as a low pass section for reference frequency components.

For the usual case where ω_{ref} is higher than $1/T_2$, the K_F function amounts to a simple resistor ratio:

$$K_F(j\omega)\Big|_{\omega = \omega_{ref}} \cong -\frac{R_2}{R_1} \qquad (14)$$

By substitution of Equations 9 and 10, this signal transfer can be related to loop parameters.

$$K_F(j\omega)\Big|_{\omega = \omega_{ref}} \cong \frac{2\zeta N\omega_n}{K_\phi K_V} = \frac{V_{ref}}{V_\phi} \qquad (15)$$

where V_{ref} = peak value of reference voltage at the VCO input, and
V_ϕ = peak value of reference frequency voltage at the phase detector output.

Sideband levels relative to reference voltage at the phase detector output can be computed by combining Equations 13 and 15:

$$\frac{\text{sideband level}}{f_{out}\text{ level}} = V_\phi \left(\frac{\zeta N\omega_n}{\omega_{ref} K_\phi}\right) \qquad (16)$$

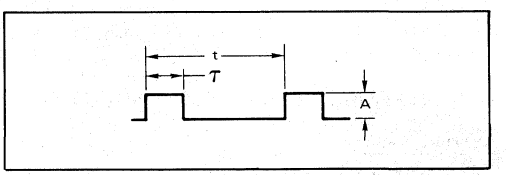
From Equation 16 we find that for a given phase detector, a given value of R_1 (which determines V_ϕ), and given basic system constraints (N, f_{ref}), only ζ and ω_n remain as variables to diminish the sidebands. If there are few limits on ω_n, it may be lowered indefinitely until the desired degree of suppression is obtained. If ω_n is not arbitrary and the sidebands are still objectionable, additional filtering is indicated.

One item worthy of note is the absence of K_V in Equation 16. From Equation 15 it might be concluded that decreasing K_V would be another means for reducing spurious sidebands, but for constant values of ζ and ω_n this is not a free variable. In a given loop, varying K_V will certainly affect sideband voltage, but will also vary ζ and ω_n.

On the other hand, the choice of ω_n may well affect spectral purity near the carrier, although reference sideband levels may be quite acceptable.

In computing sideband levels, the value of V_ϕ must be determined in relation to other loop components. Residual reference frequency components at the phase detector output are related to the dc error voltage necessary to supply charge pump leakage current and amplifier bias current. From these average voltage figures, spectral components of the reference frequency and its harmonics can be computed using an approximation that the phase detector output consists of square waves τ seconds wide repeated at t second intervals (Figure 17). A Fourier analysis can be summarized for small ratios of τ/t by:

FIGURE 17 – PHASE DETECTOR OUTPUT



(1) the average voltage (V_{avg}) is $A(\tau/t)$
(2) the peak reference voltage value (V_ϕ) is twice V_{avg}, and
(3) the second harmonic ($2f_{ref}$) is roughly equal in amplitude to the fundamental.

By knowing the requirements for (1) due to amplifier bias and leakage currents, values for (2) and (3) are uniquely determined.

An example of this sideband approximation technique can be illustrated using the parameters specified for the synthesizer design included in the applications information section.

$N_{max} = 30$ $\quad\quad$ $\omega_n = 4500$
$K_V = 11.2 \times 10^6$ rad/s/V $\quad\quad$ $R_1 = 2\ k\Omega$
$K_\phi = 0.12$ V/rad $\quad\quad$ $f_{ref} = 100$ kHz
$\zeta = 0.8$

Substituting these numbers into Equation 16:

$$\frac{\text{sideband}}{f_{out}} = V_\phi \frac{(0.8)(30)(4500)}{2\pi(10^5)(0.111)} \quad (17)$$

$$= V_\phi (1.55) \quad (18)$$

The result illustrates how much reference feedthrough will affect sideband levels. If 1.0 mV peak of reference appears at the output of the phase detector, the nearest sideband will be down 56.2 dB.

If the amplifier section included in the MC4344/4044 is used, with R_L = 1 kΩ, some approximations of the value of V_ϕ can be made based on the input bias current and the value of R_1. The phase detector must provide sufficient average voltage to supply the amplifier bias current, I_b, through R_1; when the bias current is about 5.0 μA and R_1 is 2 kΩ, V_{avg} must be 10 mV. From the assumptions earlier concerning the Fourier transform, and with the help of Figure 18, we can see that the phase detector duty cycle will be about 1.7% (A = 0.6 V), giving

FIGURE 18 – OUTPUT ERROR CHARACTERISTICS

DUTY CYCLE (%)	PHASE ERROR (Deg)	V_{avg} (mV)	$V_{\phi(peak)}$ (mV)
0.1	0.36	0.6	1.2
0.2	0.72	1.2	2.4
0.3	1.08	1.8	3.6
0.4	1.44	2.4	4.8
0.5	1.80	3.0	6.0
0.6	2.16	3.6	7.2
0.7	2.52	4.2	8.4
0.8	2.88	4.8	9.6
0.9	3.24	5.4	10.8
1.0	3.60	6.0	12.0
2.0	7.2	12.0	24.0
3.0	10.8	18.0	35.9
4.0	14.4	24.0	47.9
5.0	18.0	30.0	59.8
6.0	21.6	36.0	71.6
7.0	25.2	42.0	83.3
8.0	28.8	48.0	95.0
9.0	32.4	54.0	106.6
10.0	36.0	60.0	118.0

a fundamental (reference) of 20 mV peak. If this value for V_ϕ is substituted into Equation 18, the resulting sideband ratio represents 30 dB suppression due to this component alone.

For loop amplifiers having very high gains and relatively low bias currents, another factor to consider is reverse leakage current, I_L, of the MC4344/4044 charge pump. This is generally less than 1.0 μA although it is no more than 5.0 μA over the temperature range. A typical value for design for room temperature operation is 0.1 μA. To minimize the effects of amplifier bias and leakage currents a relatively small value of R_1 should be chosen. A minimum value of 1 kΩ is a good choice.

After values for C and R_2 have been computed on the basis of loop dynamic properties, the overall sideband to f_{out} ratio computation can be simplified.

Since

$$V_\phi = 2\,V_{avg}$$
$$V_{avg} = (I_b + I_L)\,R_1$$
$$V_\phi = 2\,(I_b + I_L)\,R_1$$
$$V_{ref} = V_\phi \left(\frac{R_2}{R_1}\right)$$
$$= 2R_1\,(I_b + I_L)\left(\frac{R_2}{R_1}\right) = 2R_2\,(I_b + I_L)$$

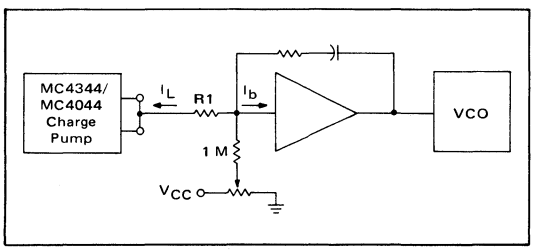
we find that

$$\frac{\text{sideband}}{f_{out}} = \frac{V_{ref} K_V}{2\omega_{ref}} \quad (19)$$

$$\frac{\text{sideband}}{f_{out}} = \frac{2R_2(I_b + I_L)K_V}{2\omega_{ref}} \quad (20)$$

Equation 20 indicates that excellent suppression could be achieved if the bias and leakage terms were nulled by current summing at the amplifier input (Figure 19). This

FIGURE 19 – COMPENSATING FOR BIAS AND LEAKAGE CURRENT



has indeed proved to be the case. Experimental results indicate that greater than 60 dB rejection can routinely be achieved at a constant temperature. However when nulling fairly large values (> 100 nA), the rejection becomes quite sensitive since leakages are inherently a function of temperature. This technique has proved useful in achieving improved system performance when used in conjunction with good circuit practice and reference filtering.

Additional Loop Filtering

So far, only the effects of fundamental loop dynamics on resultant sidebands have been considered. If further sideband suppression is required, additional loop filtering is indicated. However, care must be taken in placement of any low pass rolloff with regard to the loop natural frequency (ω_n). On one hand, the "corner" should be well below (lower than) ω_{ref} and yet far removed (above) from ω_n. Although no easy method for placing the rolloff point exists, a rule of thumb that usually works is:

$$\omega_c = 5\omega_n \quad (21)$$

Reference frequency suppression per pole is the ratio of ω_c to ω_{ref}.

$$SB_{dB} \cong n\ 20 \log_{10} \left(\frac{\omega_c}{\omega_{ref}} \right) \qquad (22)$$

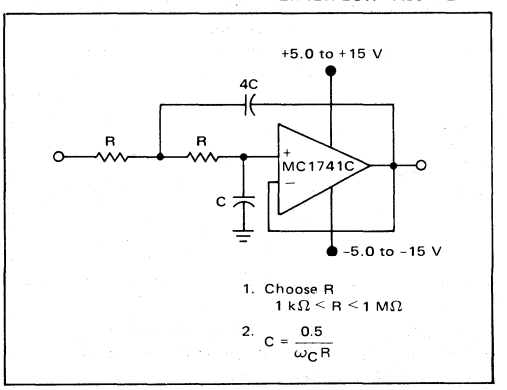
where n is the number of poles in the filter.

Equation 22 gives the additional loop suppression to ω_{ref}; this number should be added to whatever suppression already exists.

For non-critical applications, simple RC networks may suffice, but if more than one section is required, loop dynamics undergo undesirable changes. Loop damping factor decreases, resulting in a high percentage of overshoot and increased ringing since passive RC sections tend to accumulate phase shift more rapidly than signal suppression and part of this excess phase subtracts from the loop phase margin. Less phase margin translates into a lower damping factor and can, in the limit, cause outright oscillation.

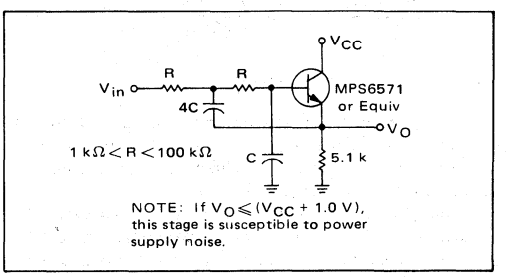
A suitable alternative is an active RC section, Figure 20,

FIGURE 20 – OPERATIONAL AMPLIFIER LOW PASS FILTER



compatible with the existing levels and voltages. An active two pole filter (second order section) can realize a more gradual phase shift at frequencies less than the cutoff point and still get nearly equal suppression at frequencies above the cutoff point. Sections designed with a slight amount of peaking ($\zeta \cong 0.5$) show a good compromise between excess phase below cutoff (ω_c), without peaking enough to cause any danger of raising the loop gain for frequencies above ω_n. A fairly non-critical section may simply use an emitter follower as the active device with two resistors and capacitors completing the circuit (Figure 21). This provides a -12 dB/octave (-40 dB/decade) rolloff characteristic above ω_n, though the attenuation may be more accurately determined by Equation 22. If the sideband problem persists, an additional section may be added in series with the first. No more than two sections are recommended since at that time either (1) the constraint

FIGURE 21 – EMITTER FOLLOWER LOW PASS FILTER

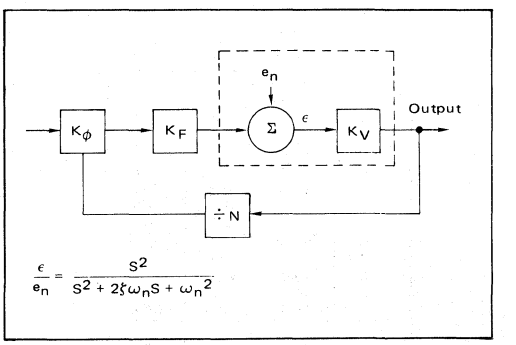


between ω_n and ω_{ref} is too close, or (2) reference voltage is modulating the VCO from a source other than the phase detector through the loop amplifier.

VCO Noise

Effects of noise within the VCO itself can be evaluated by considering a closed loop situation with an external noise source, e_n, introduced at the VCO (Figure 22). Resultant modulation of the VCO by error voltage, ϵ, is a second order high pass function:

FIGURE 22 – EFFECTS OF VCO NOISE



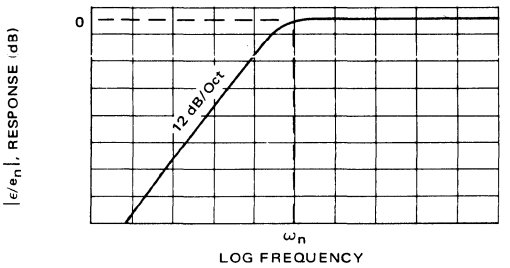
$$\frac{\epsilon}{e_n} = \frac{S^2}{S^2 + \frac{ST_2K_\phi K_V}{T_1N} + \frac{K_\phi K_V}{T_1N}} = \frac{S^2}{S^2 + 2\zeta\omega_n + \omega_n^2} \qquad (23)$$

This function has a slope of 12 dB/octave at frequencies less than ω_n (loop natural frequency), as shown in Figure 23. This means that noise components in the VCO above ω_n will pass unattenuated and those below will have some degree of suppression. Therefore choice of loop natural frequency may well rest on VCO noise quality.

Other Spurious Responses

Spurious components appearing in the output spectrum are seldom due to reference frequency feedthrough alone.

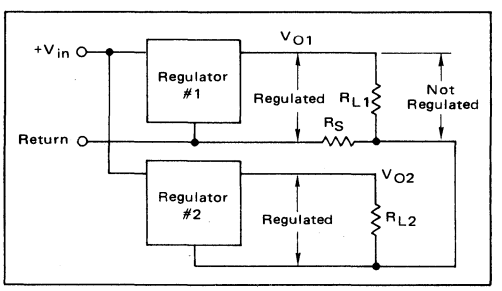
FIGURE 23 – LOOP RESPONSE TO VCO NOISE



Modulation of any kind appearing on the VCO control line will cause spurious sidebands and can come in through the loop amplifier supply, bias circuitry in the control path, a translator, or even the VCO supply itself. Some VCO's have a relatively high sensitivity to power supply variation. This should be investigated and its effects considered. Problems of this nature can be minimized by operating all devices except the phase detector, charge pump, and VCO from a separate and well isolated supply. A common method uses a master supply of about 10 or 12 volts and two regulators to produce voltages for the PLL – one for all the logic (including the phase detector) and the other for all circuitry associated with the VCO control line.

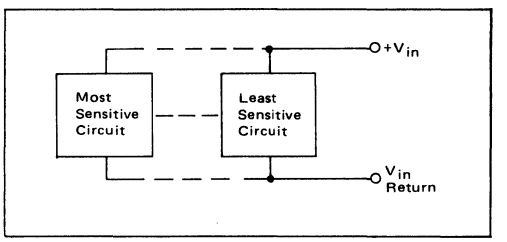
Sideband and noise performance is also a function of good power supply and regulator layout. As mentioned earlier, extreme care should be exercised in isolating the control line voltage to the VCO from influences other than the phase detector. This not only means good voltage regulation but ac bypassing and adherence to good grounding techniques as well. Figure 24 shows two separate

FIGURE 24 – LOOP VOLTAGE REGULATION



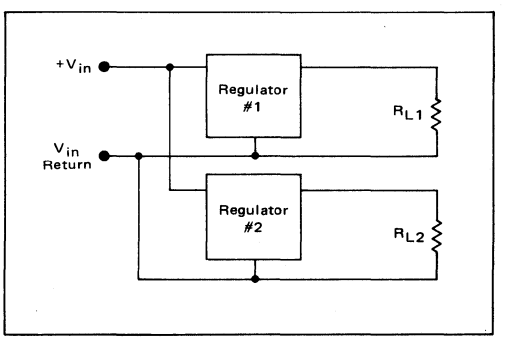
regulators and their respective loads. Resistor R_S is a small stray resistance due to a common thin ground return for both R_{L1} and R_{L2}. Any noise in R_{L2} is now reproduced (in a suppressed form) across R_{L1}. Load current from R_{L1} does not affect the voltage across R_{L2}. Even though the regulators may be quite good, they can hold V_O constant only across their outputs, not necessarily across the load (unless remote sensing is used). One solution to the ground-coupled noise problem is to lay out the return path with the most sensitive regulated circuit at the farthest point from power supply entry as shown in Figure 25.

FIGURE 25 – REGULATOR LAYOUT



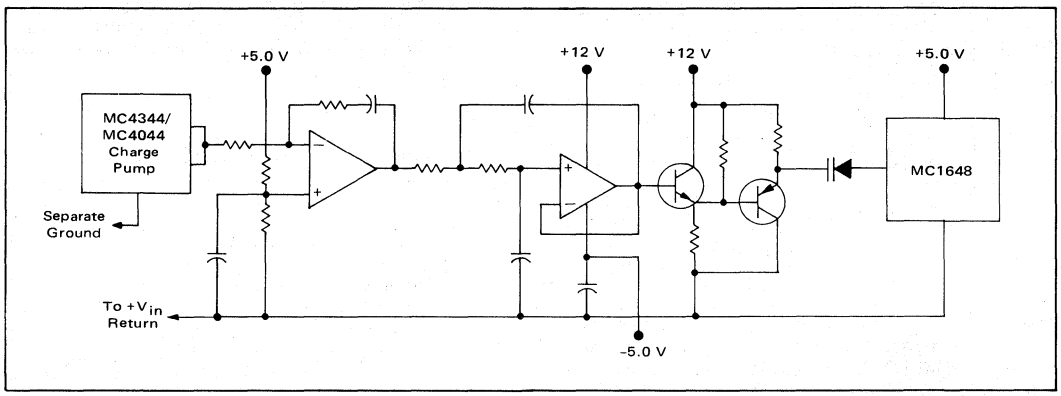
Even for regulated subcircuits, accumulated noise on the ground bus can pose major problems since although the cross currents do not produce a differential load voltage directly, they do produce essentially common mode noise on the regulators. Output differential load noise then is a function of the input regulation specification. By far the best way to sidestep the problem is to connect each subcircuit ground to the power supply entry return line as shown in Figure 26.

FIGURE 26 – REGULATOR GROUND CONNECTION



In Figures 24 and 26, R_{L1} and R_{L2} represent component groups in the system. The designer must insure that all ground return leads in a specific component group are returned to the common ground. Probably the most overlooked components are bypass capacitors. To minimize sidebands, extreme caution must be taken in the area immediately following the phase detector and through the VCO. A partial schematic of a typical loop amplifier and filter is shown in Figure 27 to illustrate the common grounding technique.

FIGURE 27 – PARTIAL SCHEMATIC OF LOOP AMPLIFIER AND FILTER



Bypassing in a phase-locked loop must be effective at both high frequencies and low frequencies. One capacitor in the 1.0-to-10 μF range and another between 0.01 and 0.001 μF are usually adequate. These can be effectively utilized both at the immediate circuitry (between supply and common ground) and the regulator if it is some distance away. When used at the regulator, a single electrolytic capacitor on the output and a capacitor pair at the input is most effective (Figure 28). It is important, again, to note that these bypasses go from the input/output pins to as near the regulator ground pin as possible.

FIGURE 28 – SUGGESTED BYPASSING PROCEDURE

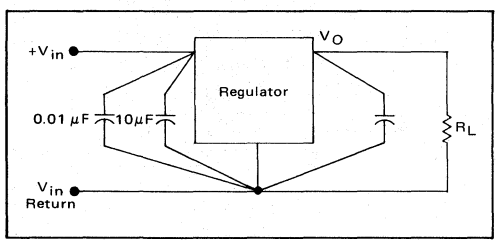
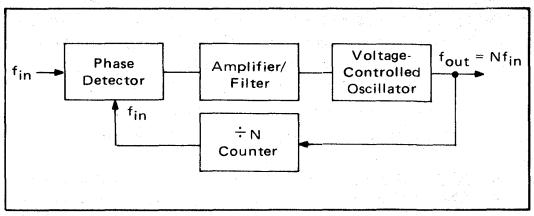


FIGURE 29 – PHASE-LOCKED LOOP WITH PROGRAMMABLE COUNTER



APPLICATIONS INFORMATION

Frequency Synthesizers

The basic PLL discussed earlier is actually a special case of frequency synthesis. In that instance, $f_{out} = f_{in}$, although normally a programmable counter in the feedback loop insures the general rule that $f_{out} = Nf_{in}$ (Figure 29). In the synthesizer f_{in} is usually constant (crystal controlled) and f_{out} is changed by varying the programmable divider (÷ N). By stepping N in integer increments, the output frequency is changed by f_{in} per increment. In communication use, this input frequency is called the "channel spacing" or, in general, it is the reference frequency.

There is essentially no difference in loop dynamic problems between the basic PLL and synthesizers except that synthesizer designers must contend with problems peculiar to loops where N is variable and greater than 1. Also, sidebands or spectral purity usually require special attention. These and other aspects are discussed in greater detail in AN-535. The steps for a suitable synthesis procedure may be summarized as follows:

Synthesis Procedure

1. Choose input frequency. (f_{ref} = channel spacing)
2. Compute the range of digital division:

$$N_{max} = \frac{f_{max}}{f_{ref}}$$

$$N_{min} = \frac{f_{min}}{f_{ref}}$$

3. Compute needed VCO range:

$$(2f_{max} - f_{min}) < f_{VCO} < (2f_{min} - f_{max})$$

4. Choose minimum ζ from transient response plot, Figure 9. A good starting point is $\zeta = 0.5$.

5. Choose ω_n from needed response time (Figure 9):

$$\omega_n = \frac{\omega_n t}{t}$$

6. Compute C:

$$C = \frac{K_\phi K_V}{N_{max}\omega_n^2 R_1}$$

7. Compute R_2:

$$R_2 = \frac{2\zeta_{min}}{\omega_n C}$$

8. Compute ζ_{max}:

$$\zeta_{max} = \zeta_{min}\sqrt{\frac{N_{max}}{N_{min}}}$$

9. Check transient response of ζ_{max} for compatibility with transient specification.
10. Compute expected sidebands:

$$\frac{\text{sideband}}{f_{out}} \cong \frac{(I_b + I_L)R_2 K_V}{\omega_{ref}} \qquad \text{(A)}$$

(I_L is about 100 nA at $T_J = 25^oC$.)

11. If step 10 yields larger sidebands than are acceptable, add a single pole at the loop amplifier by splitting R_1 and adding C_c as shown in Figure 15:

$$C_c \cong \frac{0.8}{R_1\omega_n}$$

Added sideband suppression (dB) is:

$$dB \cong 20\log_{10}\frac{1}{\sqrt{1+\frac{\omega_{ref}^2}{25(\omega_n)^2}}} \qquad \text{(B)}$$

12. If step 11 still does not give the desired results, add a second order section at $\omega_c = 5\ \omega_n$ using either the configuration of Figure 20 or 21. The expected improvement is twice that of the single pole in step 10.

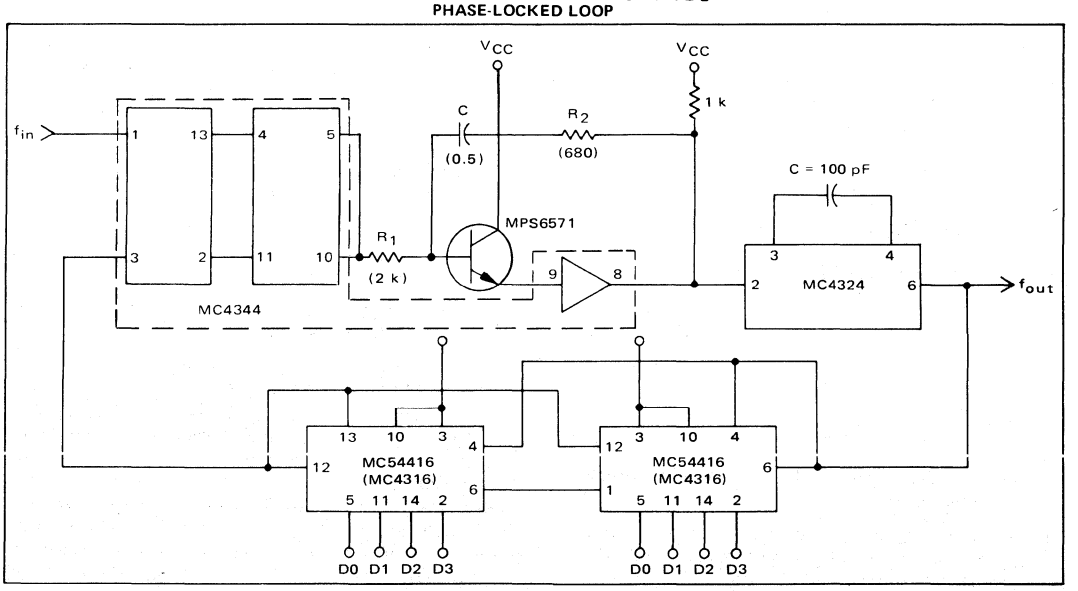
$$dB \cong 40\log_{10}\frac{1}{\sqrt{1+\frac{\omega_{ref}^2}{25(\omega_n)^2}}} \qquad \text{(C)}$$

Total sideband rejection is then the total of $20\log_{10}$(A) + (B) + (C).

Design Example (Figure 30)

Assume the following requirements:
Output frequency, f_{out} = 2.0 MHz to 3.0 MHz
Frequency steps, f_{in} = 100 kHz

FIGURE 30 – CIRCUIT DIAGRAM OF TYPE 2 PHASE-LOCKED LOOP



Lockup time between channels (to 5%) = 1.0 ms
Overshoot < 20%.
Minimum sideband suppression = -30 dB

From the steps of the synthesis procedure:

1. $f_{ref} = f_{in} = 100\ kHz$

2. $N_{max} = \frac{f_{max}}{f_{ref}} = \frac{3.0\ MHz}{0.1\ MHz} = 30$

   $N_{min} = \frac{f_{min}}{f_{ref}} = \frac{2.0\ MHz}{0.1\ MHz} = 20$

3. VCO range:
   The VCO output frequency range should extend beyond the specified minimum-maximum limits to accommodate the overshoot specification. In this instance f_{out} should be able to cover an additional 20% on either end. End limits on the VCO are:

   $f_{out}max \geq 3.0 + 0.2(3.0) = 3.6\ MHz$
   $f_{out}min \leq 2.0 - 0.2(2.0) = 1.6\ MHz$

   This VCO range ($\approx 2.25:1$) is realizable with the MC4324/4024 voltage controlled multivibrator. From Figure 7 of the MC4324/4024 data sheet we find the required tuning capacitor value to be 120 pF and the VCO gain, K_V, typically 11×10^6 rad/s/v.

4. From the step response curve of Figure 5, $\zeta = 0.8$ will produce a peak overshoot less than 20%.

5. Referring to Figure 9, overshoot with $\zeta = 0.8$ will settle to within 5% at $\omega_n t = 4.5$. Since the required lock-up time is 1.0 ms,

   $$\omega_n = \frac{\omega_n t}{t} = \frac{4.5}{t} = \frac{4.5}{0.001} = (4.5)(10^3)\ rad/s$$

6. In order to compute C, phase detector gain and R1 must be selected. Phase detector gain, K_ϕ, for the MC4344/4044 is approximately 0.1 volt/radian with $R_1 = 1\ k\Omega$. Therefore,

   $$C = \frac{(0.1)(11 \times 10^6)}{(30)(4.5 \times 10^3)^2(10^3)} = 2.0\ \mu F$$

7. At this point, R_2 can be computed:

   $$R_2 = \frac{2\zeta_{min}}{\omega_n C} = \frac{1.6}{(4.5 \times 10^3)(2 \times 10^{-6})} = 180\ \Omega$$

8. $$\zeta_{max} = \zeta_{min}\sqrt{\frac{N_{max}}{N_{min}}} = 0.98$$

9. Figure 9 shows that $\zeta = 0.98$ will meet the settling time requirement.

10. Sidebands may be computed for two cases: (1) with I_L (charge pump leakage current) nominal (100 nA), and (2) with I_L maximum (5.0 μA).

    $$\left.\frac{\text{sideband}}{f_{out}}\right|_{max} = \frac{(5 \times 10^{-6})(180)(11 \times 10^6)}{4.5 \times 10^3} \cong 2.2$$

    Since I_L (nominal) is 50 times lower than I_L (maximum), the sideband-to-center frequency ratio nominally would be:

    $$\left.\frac{\text{sideband}}{f_{out}}\right|_{nom} = \frac{2.2}{50} = 0.044$$

    $$= 20\log_{10}(0.044) \cong -27\ dB$$

    This suppression figure does not meet the original design requirement. Therefore further improvements will be made.

11. By splitting R_1 and C_c, further attenuation can be gained. The magnitude of C_c is approximately:

    $$C_c \cong \frac{0.8}{R_1\omega_n} = \frac{0.8}{(10^3)(4.5)(10^3)} \cong 0.2\ \mu F$$

    Improvement in sidebands will be:

    $$20\log_{10}\frac{1}{1 + \frac{105^2}{25(4.5 \times 10^3)^2}} = -13\ dB$$

    Nominal suppression is now -40 dB. Worst-case is 34 dB higher than nominal suppression (50:1 ratio), or -6.0 dB. Therefore additional filtering is required.

12. Additional filters such as second order sections are exactly double the single order sections as designed in step 11. Adding such a filter would give an additional -26 dB rejection factor. Therefore, one second order filter section would result in an overall sideband suppression of -67 dB nominal and -32 dB maximum.

Design of the passive components for the added section with R assigned a value of 10 kΩ is:

$$C = \frac{0.1}{\omega_n R} = \frac{0.1}{(4.5 \times 10^{-3})(10^4)} = 0.2\ \mu F$$

See Figures 20 and 21 for two configurations that will satisfy this filter requirement.

Clock Recovery from Phase-Encoded Data

The electro-mechanical system used for recording digital data on magnetic tape often introduces random variations in tape speed and data spacing. Because of this and the encoding technqiue used, it is usually necessary to regenerate a synchronized clock from the data during this read cycle. One method for doing this is to phase-lock a voltage controlled multivibrator to the data as it is read (Figure 31).

FIGURE 31 – CLOCK RECOVERY FROM PHASE-ENCODED DATA

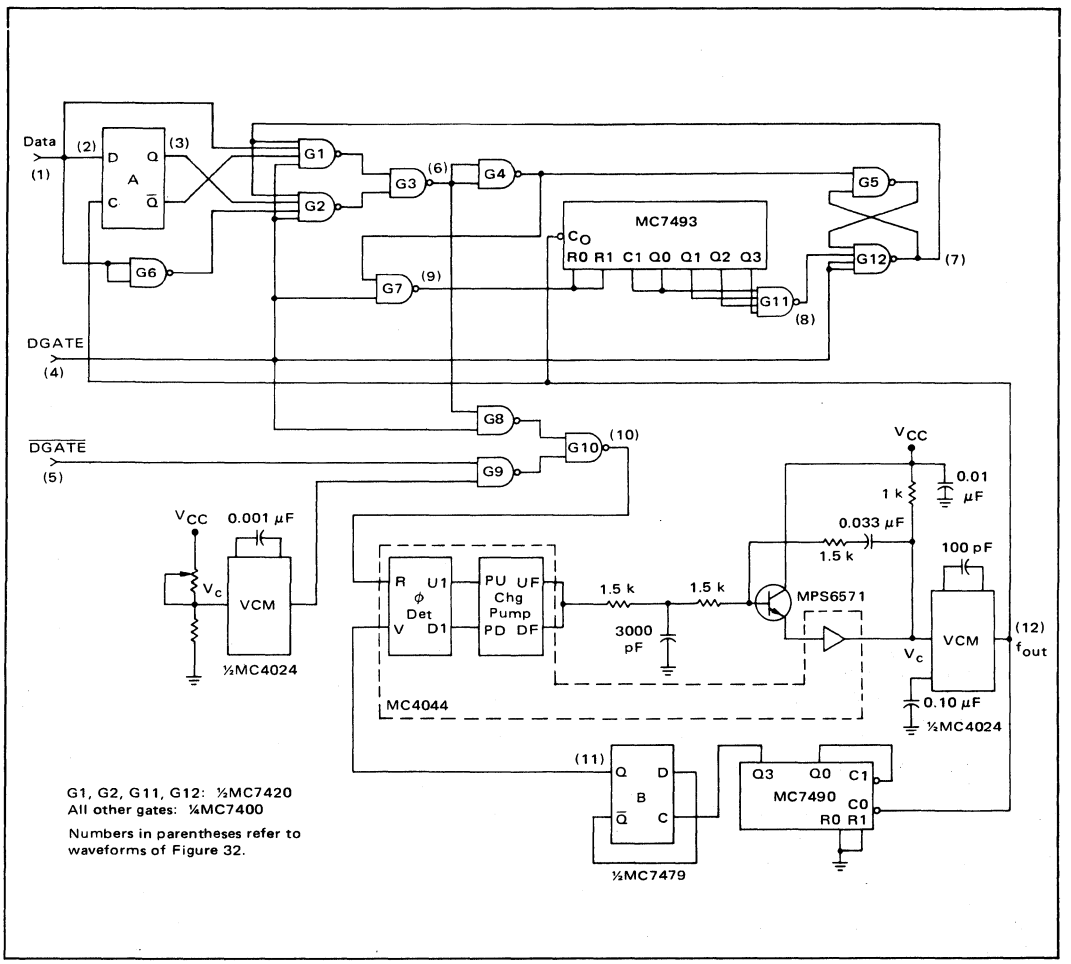
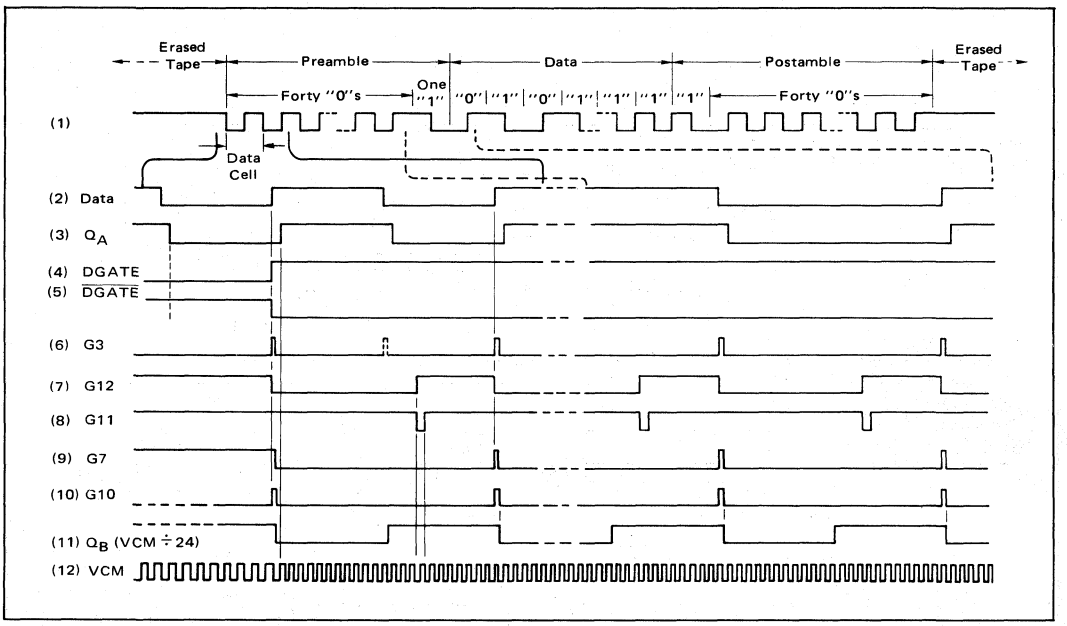


FIGURE 32 – TIMING DIAGRAM – CLOCK RECOVERY FROM PHASE-ENCODED DATA



A typical data block using the phase encoded format is shown in row 1 of Figure 32. The standard format calls for recording a preamble of forty "0"s followed by a single "1"; this is followed by from 18 to 2048 characters of data and a postamble consisting of a "1" followed by forty "0"s. The encoding format records a "0" as a transition from low to high in the middle of a data cell. A "1" is indicated by a transition from high to low at the data cell midpoint. When required, phase transitions occur at the end of data cells. If a string of either consecutive "0"s or consecutive "1"s is recorded, the format duplicates the original clock; the clock is easily recovered by straight forward synchronization with a phase-locked loop. In the general case, where the data may appear in any order, the phase-encoded data must be processed to obtain a single pulse during each data cell before it is applied to the phase detector. For example, if the data consisted only of alternating "1"s and "0"s, the phase-encoded format would result in a waveform equal to one-half the original clock frequency. If this were applied directly to the loop, the VCM would of course move down to that frequency. The encoding format insures that there will be a transition in the middle of each data time. If only these transitions are sensed they can be used to regenerate the clock. The schematic diagram of Figure 31 indicates one method of accomplishing this.

The logic circuitry generates a pulse at the midpoint of each data cell which is then applied to the reference input of the phase detector. The loop VCM is designed to operate at some multiple of the basic clock rate. The VCM frequency selected depends on the decoding resolution desired and other system timing requirements. In this example, the VCM operates at twenty-four times the clock rate (Figure 32, Row 12).

Referring to Figure 31 and the timing diagram of Figure 32, the phase-encoded data (Figure 32, Row 1) is combined with a delayed version of itself (output of flip-flop A row 3) to provide a positive pulse out of G3 for every transition of the input signal. Portions of the data block are shown expanded in row 2 of Figure 32. Flip-flop A delays the incoming data of one-half of a VCM clock period. Gates G1, G2, and G3 implement the logic Exclusive OR of waveforms 1 and 3 except when inhibited by DGATE (row 4) or the output of G12 (row 7). DGATE and its complement, $\overline{DGATE}$, serve to initialize the circuitry and insure that the first transition of the data block (a phase transition) is ignored. The MC7493 binary counter and the G5-G12 latch generate a suitable signal for gating out G3 pulses caused by phase transitions at the end of a data cell, such as the one shown dashed in row 6.

The initial data pulse from G3 sets G12 low and is combined with DGATE in G7 to reset the counter to its zero state. Subsequent VCM clock pulses now cycle the counter and approximately one-third of the way through the next data cell the counter's full state is decoded by G11, generating a negative transition. This causes G12 to go high, removing the inhibit signal until it is again reset by the next data transition. This pulse also resets the

counter, continuing the cycle and generating a positive pulse at the midpoint of each data cell as required.

Acquisition time is reduced if the loop is locked to a frequency approximately the same as the expected data rate during inter-block gaps. In Figure 31, this is achieved by operating the remaining half of the dual VCM at slightly less than the data rate and applying it to the reference input of the phase detector via the G8-G9-G10 data selector. When data appears, DGATE and $\overline{\text{DGATE}}$ cause the output of G3 to be selected as the reference input to the loop.

The loop parameters are selected as a compromise between fast acquisition and jitter-free tracking once synchronization is achieved. The resulting filter component values indicated in Figure 31 are suitable for recovering the clock from data recorded at a 120 kHz rate, such as would result in a tape system operating at 75 i.p.s. with a recording density of 1600 b.p.i. Synchronization is achieved by approximately the twenty-fourth bit time of the preamble. The relationship between system requirements and the design procedure is illustrated by the following sample calculation:

Assume a -3.0 dB loop bandwidth much less than the input data rate ($\approx$ 120 kHz), say 10 kHz. Further, assume a damping factor of $\zeta = 0.707$. From the expression for loop bandwidth as a function of damping factor and undamped natural frequency, ω_n, calculate ω_n as:

$$\omega_{-3\text{ dB}} = \omega_n \left(1 + 2\zeta^2 + \sqrt{2 + 4\zeta^2 + 4\zeta^4}\right)^{1/2} \quad (24)$$

or for $\omega_{-3\text{ dB}} = (2\pi)10^4$ rad/s and $\zeta = 0.707$:

$$\omega_n = \frac{(2\pi)10^4}{2.06} = (3.05)10^4 \text{ rad/s}$$

As a rough check on acquisition time, assume that lockup should occur not later than half-way through a 40-bit preample, or for twenty 8.34 μs data periods.

$$\omega_n t = (3.05)10^4\,(20)(8.34)10^{-6} = 5.1 \quad (26)$$

From Figure 9, the output will be within 2 to 3% of its final value for $\omega_n t \approx 5$ and $\zeta = 0.707$. The filter components are calculated by:

$$\frac{K_\phi K_V}{R_1 CN} = \omega_n^2 \quad (27)$$

and

$$\frac{K_\phi K_V R_2}{R_1 N} = 2\zeta\omega_n \quad (28)$$

where $K_\phi = 0.015$ v/rad
$K_V = (18.2)10^6$ rad/s/volt
$N = 24$ = Feedback divider ratio
$\omega_n = (3.05)10^4$ rad/s
$\zeta = 0.707$

$$\frac{K_\phi K_V}{N} = \frac{(0.115)(18.2)10^6}{24} = (8.72)10^4$$

From Equation 27:

$$R_1 C = \frac{K_\phi K_V}{N\omega_n^2} = \frac{(8.72)10^4}{(3.05)^2 10^8} = (9.34)10^{-5}$$

From Equation 28:

$$\frac{R_2}{R_1} = \frac{2\zeta\omega_n N}{K_\phi K_V} = \frac{2(0.707)(3.04)10^4}{(8.72)10^4} = 0.494 \approx \tfrac{1}{2}$$

Let $R_1 = 3.0$ kΩ; then $R_2 = 1.5$ kΩ and

$$C = \frac{(9.34)10^{-5}}{(3.0)10^3} = (3.1)10^{-8}$$

or using a close standard value, use $C = 0.0033\,\mu$F. Now add the additional prefiltering by splitting R_1 and selecting a time constant for the additional section so that it is large with respect to R_2C_2.

$$10(\tfrac{1}{2}R_1)C_s = R_2 C$$

or

$$C_s = \frac{2R_2C}{10R_1} = \frac{2(1.5)10^3(3.3)10^{-8}}{10(3.0)10^3} = 3300 \text{ pF}$$

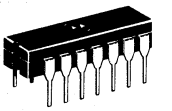
PHASE-FREQUENCY DETECTOR

MC12040

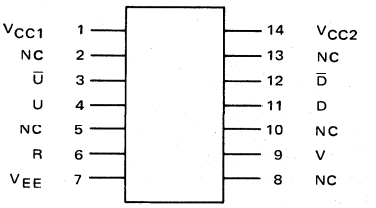
2

The MC12040 is a phase-frequency detector intended for use in systems requiring zero phase and frequency difference at lock. In combination with a voltage controlled oscillator (such as the MC1648), it is useful in a broad range of phase-locked loop applications. Operation of this device is identical to that of Phase Detector #1 of the MC4044. A discussion of the theory of operation and applications information is given on the MC4344/4044 data sheet.

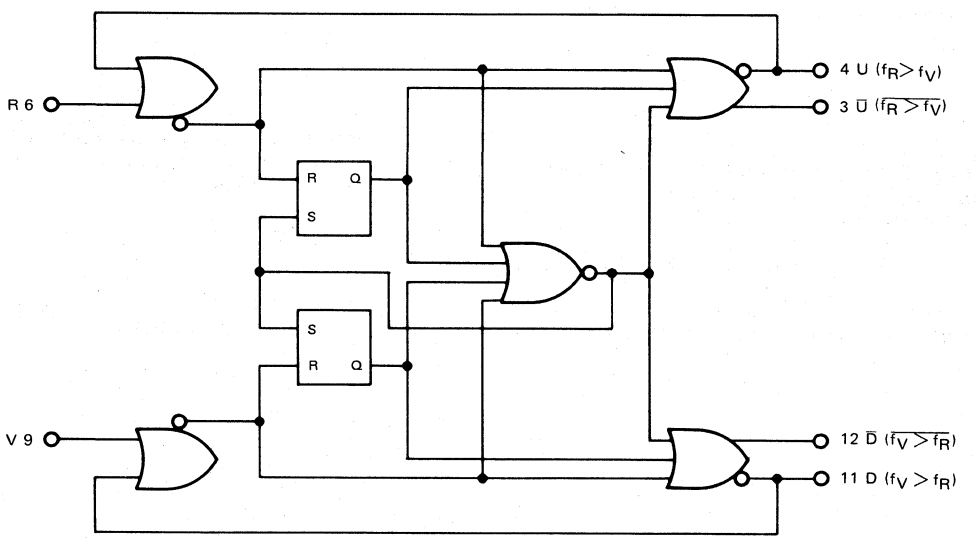
- Operating Frequency = 80 MHz typical



CERAMIC PACKAGE
CASE 632-02



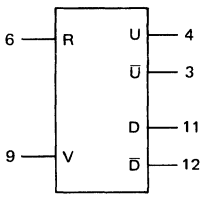
NC – No Connection



V_{CC1} = Pin 1
V_{CC2} = Pin 14
V_{CC3} = Pin 7

ELECTRICAL CHARACTERISTICS

The MC12040 has been designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 50 ohm resistor to +3.0 V for +5.0 V tests and through a 50 ohm resistor to -2.0 V for -5.2 V tests.



INPUT		OUTPUT			
R	V	U	D	Ū	D̄
0	0	X	X	X	X
0	1	X	X	X	X
1	1	X	X	X	X
0	1	X	X	X	X
1	1	1	0	0	1
0	1	1	0	0	1
1	1	1	0	0	1
1	0	1	0	0	1
1	1	0	0	1	1
1	0	0	0	1	1
1	1	0	1	1	0
1	0	0	1	1	0
1	1	0	1	1	0
0	1	0	1	1	0
1	1	0	0	1	0

X = Don't Care

TRUTH TABLE

This is not strictly a functional truth table; i.e., it does not cover all possibile modes of operation. However it gives a sufficient number of tests to ensure that the device will function properly in all modes of operation.

Supply Voltage = -5.2V

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
25°C	-0.810	-1.850	-1.105	-1.475	-5.2
75°C	-0.720	-1.830	-1.045	-1.450	-5.2

Characteristic	Symbol	Pin Under Test	MC12040 0°C Min	0°C Max	25°C Min	25°C Typ	25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	7	–	–	-60	-90	-120	–	–	mAdc	–	–	–	–	7	1,14
Input Current	I_{INH}	6	–	–	–	–	350	–	–	µAdc	6	–	–	–	7	1,14
		9	–	–	–	–	350	–	–	µAdc	9	–	–	–	7	1,14
	I_{INL}	6	–	–	0.5	–	–	–	–	µAdc	–	6	–	–	7	1,14
		9	–	–	0.5	–	–	–	–	µAdc	–	9	–	–	7	1,14
Logic "1" Output Voltage	V_{OH} ①	3	-1.000	-0.840	-0.960	–	-0.810	-0.900	-0.720	Vdc	–	–	–	–	7	1,14
		4	↓	↓	↓	–	↓	↓	↓	↓	–	–	–	–	↓	↓
		11				–					–	–	–	–		
		12				–					–	–	–	–		
Logic "0" Output Voltage	V_{OL} ①	3	-1.870	-1.635	-1.850	–	-1.620	-1.830	-1.595	Vdc	–	–	–	–	7	1,14
		4	↓	↓	↓	–	↓	↓	↓	↓	–	–	–	–	↓	↓
		11				–					–	–	–	–		
		12				–					–	–	–	–		
Logic "1" Threshold Voltage	V_{OHA} ②	3	-1.020	–	-0.980	–	–	-0.920	–	Vdc	–	–	6.9	–	7	1,14
		4	↓	–	↓	–	–	↓	–	↓	–	–	↓	–	↓	↓
		11		–		–	–		–		–	–		–		
		12		–		–	–		–		–	–		–		
Logic "0" Threshold Voltage	V_{OLA} ②	3	–	-1.615	–	–	-1.600	–	-1.575	Vdc	–	–	9	6	7	1,14
		4	–	↓	–	–	↓	–	↓	↓	–	–	6	9	↓	↓
		11	–		–	–		–			–	–	9	6		
		12	–		–	–		–			–	–	6	9		

Supply Voltage = +5.0V

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{CC}
0°C	+4.160	+3.130	+3.855	+3.510	+5.0
25°C	+4.190	+3.150	+3.895	+3.525	+5.0
75°C	+4.280	+3.170	+3.955	+3.550	+5.0

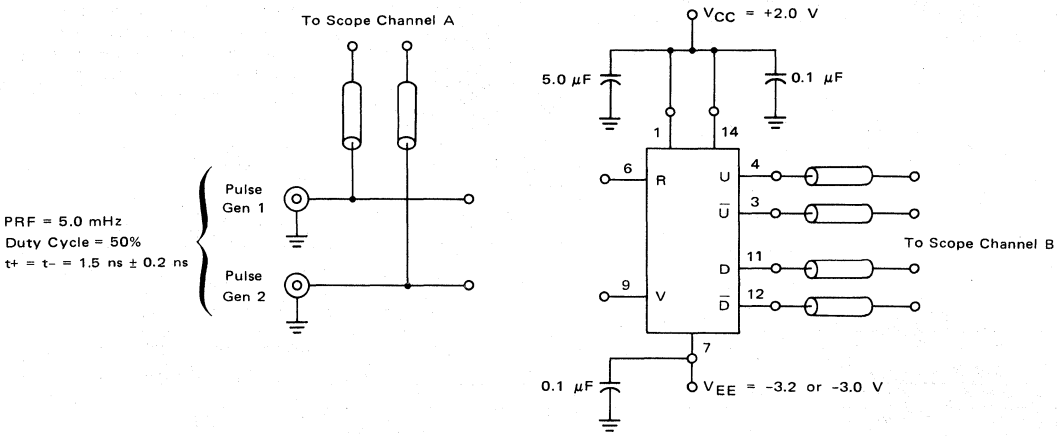
Characteristic	Symbol	Pin Under Test	MC12040 0°C Min	0°C Max	25°C Min	25°C Typ	25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{CC}	(V_{EE}) Gnd
Power Supply Drain Current	I_E	7	–	–	-60	-85	-115	–	–	mAdc	–	–	–	–	1,14	7
Input Current	I_{INH}	6	–	–	–	–	350	–	–	µAdc	6	–	–	–	1,14	7
		9	–	–	–	–	350	–	–	µAdc	9	–	–	–	1,14	7
	I_{INL}	6	–	–	0.5	–	–	–	–	µAdc	–	6	–	–	1,14	7
		9	–	–	0.5	–	–	–	–	µAdc	–	9	–	–	1,14	7
Logic "1" Output Voltage	V_{OH} ①	3	4.000	4.160	4.040	–	4.190	4.100	4.280	Vdc	–	–	–	–	1,14	7
		4	↓	↓	↓	–	↓	↓	↓	↓	–	–	–	–	↓	↓
		11				–					–	–	–	–		
		12				–					–	–	–	–		
Logic "0" Output Voltage	V_{OL} ①	3	3.190	3.430	3.210	–	3.440	3.230	3.470	Vdc	–	–	–	–	1,14	7
		4	↓	↓	↓	–	↓	↓	↓	↓	–	–	–	–	↓	↓
		11				–					–	–	–	–		
		12				–					–	–	–	–		
Logic "1" Threshold Voltage	V_{OHA} ②	3	3.980	–	4.020	–	–	4.080	–	Vdc	–	–	6.9	–	1,14	7
		4	↓	–	↓	–	–	↓	–	↓	–	–	↓	–	↓	↓
		11		–		–	–		–		–	–		–		
		12		–		–	–		–		–	–		–		
Logic "0" Threshold Voltage	V_{OLA} ②	3	–	3.450	–	–	3.460	–	3.490	Vdc	–	–	9	6	1,14	7
		4	–	↓	–	–	↓	–	↓	↓	–	–	6	9	↓	↓
		11	–		–	–		–			–	–	9	6		
		12	–		–	–		–			–	–	6	9		

① Outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests.

② The device must also function according to the truth table during these tests.

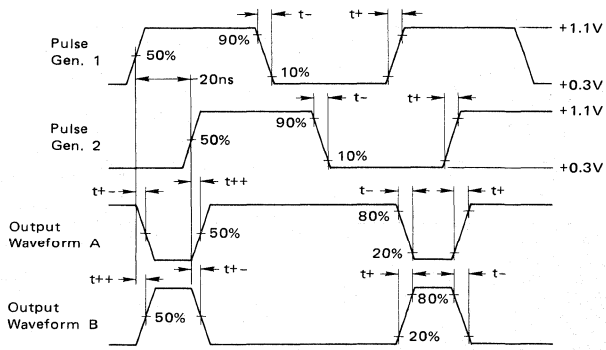
2

AC TESTS



NOTES:

1. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable.
2. Unused input and outputs are connected to a 50 Ω resistor to ground.
3. The device under test must be preconditioned before performing the ac tests. Preconditioning may be accomplished by applying pulse generator 1 for a minimum of two pulses prior to pulse generator 2. The device must be preconditioned again when inputs to pins 6 and 9 are interchanged. The same technique applies.



Characteristic	Symbol	Pin Under Test	Output Waveform	MC12040 0°C Min	MC12040 0°C Max	MC12040 +25°C Min	MC12040 +25°C Typ	MC12040 +25°C Max	MC12040 +75°C Min	MC12040 +75°C Max	Unit	TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW: Pulse Gen. 1	Pulse Gen. 2	VEE -3.0 or -3.2 V	VCC +2.0 V
Propagation Delay	t_{6+4+}	6,4	B	1.6	2.8	1.6	–	2.8	1.6	3.8	ns	6	9	7	1,14
	t_{6+12+}	6,12	A	2.6	4.0	2.6	–	4.0	2.6	5.2		9	6		
	t_{6+3-}	6,3	A	1.6	2.8	1.6	–	2.8	1.6	3.8		6	9		
	t_{6+11-}	6,11	B	2.8	4.2	2.8	–	4.2	2.8	5.5		9	6		
	t_{9+11+}	9,11	B	1.6	2.8	1.6	–	2.8	1.6	3.8		9	6		
	t_{9+3+}	9,3	A	2.6	4.0	2.6	–	4.0	2.6	5.2		6	9		
	t_{9+12-}	9,12	A	1.6	2.8	1.6	–	2.8	1.6	3.8		9	6		
	t_{9+4-}	9,4	B	2.8	4.2	2.8	–	4.2	2.8	5.5		6	9		
Output Rise Time	t_{3+}	3	A	0.8	2.1	0.8	1.5	2.1	0.8	2.8	ns	6	9	7	1,14
	t_{4+}	4	B									6	9		
	t_{11+}	11	B									9	6		
	t_{12+}	12	A									9	6		
Output Fall Time	t_{3-}	3	A	0.8	2.1	0.8	1.5	2.1	0.8	2.8	ns	6	9	7	1,14
	t_{4-}	4	B									6	9		
	t_{11-}	11	B									9	6		
	t_{12-}	12	A									9	6		

APPLICATIONS INFORMATION

The MC12040 is a logic network designed for use as a phase comparator for MECL-compatible input signals. It determines the "lead" or "lag" phase relationship and the time difference between the leading edges of the waveforms. Since these edges occur only once per cycle, the detector has a range of $\pm 2\pi$ radians.

Operation of the device may be illustrated by assuming two waveforms, R and V (Figure 1), of the same frequency but differing in phase. If the logic had established by past history that R was leading V, the U output of the detector (pin 4) would produce a positive pulse width equal to the phase difference and the D output (pin 11) would simply remain low.

On the other hand, it is also possible that V was leading R (Figure 1), giving rise to a positive pulse on the D output and a constant low level on the U output pin. Both outputs for the sample condition are valid since the determination of lead or lag is dependent on past edge crossing and initial conditions at start-up. A stable phase-locked loop will result from either condition.

Phase error information is contained in the output duty cycle – that is, the ratio of the output pulse width to total period. By integrating or low-pass filtering the outputs of the detector and shifting the level to accommodate ECL swings, usable analog information for the voltage-controlled oscillator can be developed. A circuit useful for this function is shown in Figure 2.

Proper level shifting is acomplished by differentially driving the operational amplifier from the normally high outputs of the phase detector ($\overline{U}$ and $\overline{D}$). Using this technique the quiescent differential voltage to the operational amplifier is zero (assuming matched "1" levels from the phase detector). The $\overline{U}$ and $\overline{D}$ outputs are then used to pass along phase information to the operational amplifier. Phase error summing is accomplished through resistors R1 connected to the inputs of the operational amplifier. Some R-C filtering imbedded within the input network (Figure 2) may be very beneficial since the very narrow correctional pulses of the MC12040 would not normally be integrated by the amplifier. General design guides for calculating R1, R2, and C are included in the MC4044 data sheet. Phase detector gain for this configuration is approximately 0.16 volts/radian.

System phase error stems from input offset voltage in the operational amplifier, mismatching of nominally equal resistors, and mismatching of phase detector "high" states between the outputs used for threshold setting and phase measuring. All these effects are reflected in the gain constant. For example, a 16 mV offset voltage in the amplifier would cause an error of 0.016/0.16 = 0.1 radian or 5.7 degrees of error. Phase error can be trimmed to zero initially by trimming either input offset or one of the threshold resistors (R1 in Figure 2). Phase error over temperature depends on how much the offending parameters drift. If better performance were desired, the "charge pump" concept of the MC4044 could be implemented and subsequent errors could be reduced considerably since offsets no longer enter the picture.

FIGURE 1 – TIMING DIAGRAM

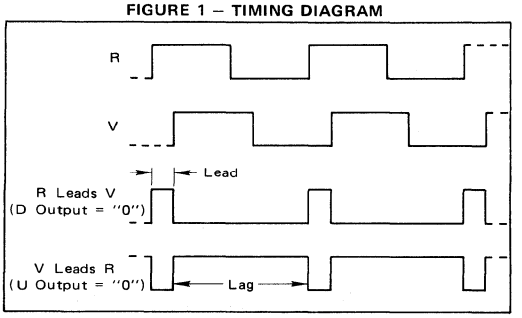
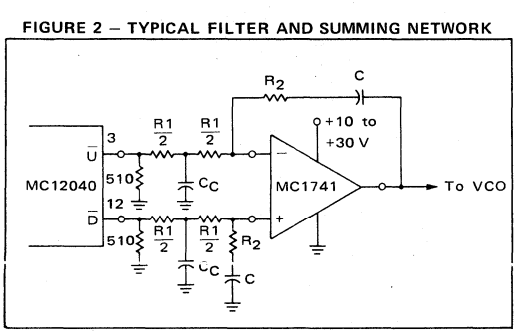
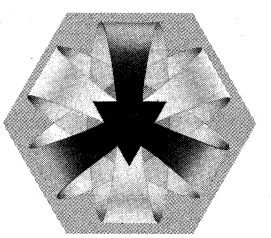


FIGURE 2 – TYPICAL FILTER AND SUMMING NETWORK

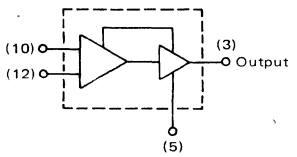


OSCILLATORS-MULTIVIBRATORS

3



MC1648



Numbers in parenthesis denote pin number for F package (Case 607) L package (Case 632), and P package (Case 646).

Input Capacitance = 6 pF typ
Maximum Series Resistance for L (External Inductance) = 50 Ω typ
Power Dissipation = 150 mW typ/pkg (+5.0 Vdc Supply)
Maximum Output Frequency = 225 MHz typ

The MC1648 is an emitter-coupled oscillator, constructed on a single monolithic silicon chip. Output levels are compatible with MECL III logic levels. The oscillator requires an external parallel tank circuit consisting of the inductor (L) and capacitor (C).

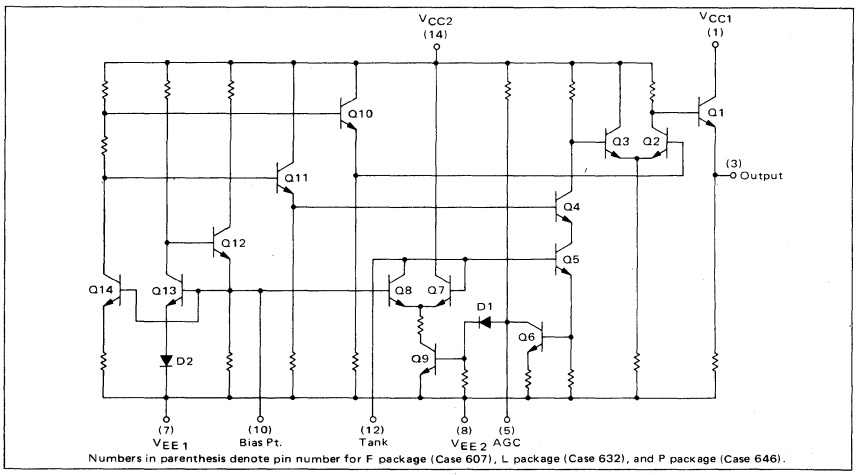
A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). The MC1648 was designed for use in the Motorola Phase-Locked Loop shown in Figure 9. This device may also be used in many other applications requiring a fixed or variable frequency clock source of high spectral purity (See Figure 2).

The MC1648 may be operated from a +5.0 Vdc supply or a -5.2 Vdc supply, depending upon system requirements.

SUPPLY VOLTAGE	GND PINS	SUPPLY PINS
+5.0 Vdc	7, 8	1, 14
-5.2 Vdc	1, 14	7, 8

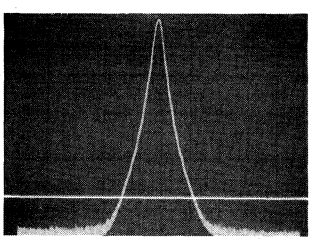
3

FIGURE 1 – CIRCUIT SCHEMATIC



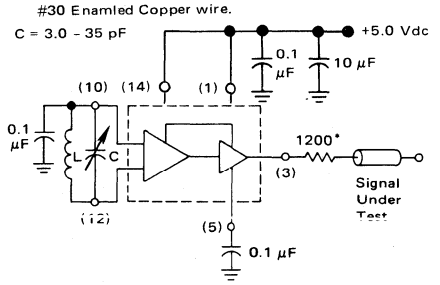
Numbers in parenthesis denote pin number for F package (Case 607), L package (Case 632), and P package (Case 646).

FIGURE 2 – SPECTRAL PURITY OF SIGNAL AT OUTPUT



B.W. = 10 kHz
Center Frequency = 100 MHz
Scan Width = 50 kHz/div
Vertical Scale = 10 dB/div

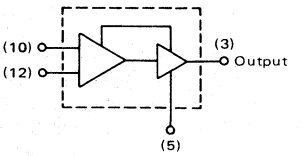
L: Micro Metal toroid #T20-13, 8 turns
#30 Enamled Copper wire.
C = 3.0 - 35 pF



*The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

ELECTRICAL CHARACTERISTICS

Supply Voltage = +5.0 volts



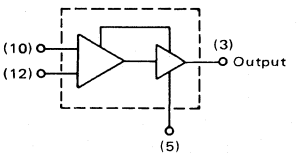
@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts) V_{IH} max	V_{IL} min	V_{CC}	mAdc I_L
0°C	+1.900	+1.400	5.0	-5.0
+25°C	+1.800	+1.300	5.0	-5.0
+75°C	+1.700	+1.200	5.0	-5.0

Characteristic	Symbol	Pin Under Test	MC1648 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{CC}	I_L	V_{EE} (Gnd)
Power Supply Drain Current	I_E	8	–	–	–	35	–	–	mAdc	–	–	1, 14	–	7, 8
Logic "1" Output Voltage	V_{OH}	3	4.00	4.16	4.04	4.19	4.10	4.28	Vdc	–	12	1, 14	3	7, 8
Logic "0" Output Voltage	V_{OL}	3	3.18	3.42	3.20	3.43	3.22	3.46	Vdc	12	–	1, 14	3	7, 8
Bias Voltage	V_{Bias}*	10	1.45	1.8	1.4	1.7	1.3	1.6	Vdc	–	–	1, 14	–	7, 8
			Min	Typ Max	Min	Typ Max	Min	Typ Max						
Peak-to-Peak Tank Voltage	V_{p-p}	12	–	– –	–	500 –	–	– –	mV	See Figure 3	–	1, 14	3	7, 8
Output Duty Cycle	V_{DC}	3	–	– –	–	50 –	–	– –	%	See Figure 3	–	1, 14	3	7, 8
Oscillation Frequency	f_{max}	–	–	– –	195	225 –	–	– –	MHz	See Figure 3	–	1, 14	3	7, 8

*This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor tuning diode at this point.

ELECTRICAL CHARACTERISTICS

Supply Voltage = -5.2 volts

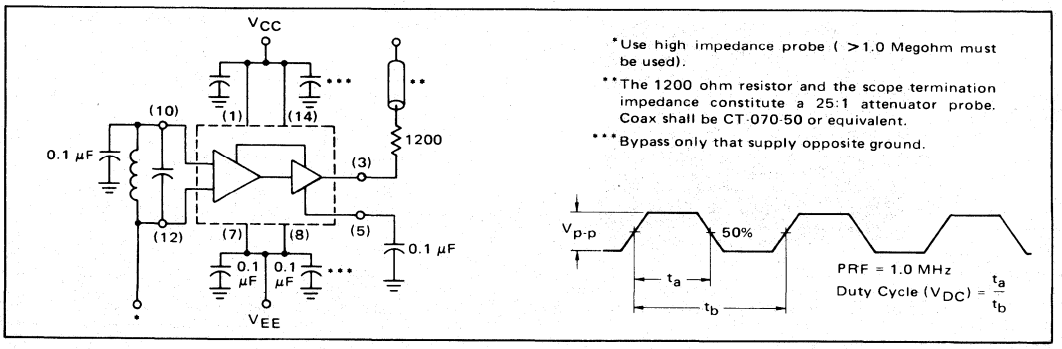


@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts) V_{IH} max	V_{IL} min	V_{EE}	mAdc I_L
0°C	-3.300	-3.800	-5.2	-5.0
+25°C	-3.400	-3.900	-5.2	-5.0
+75°C	-3.500	-4.000	-5.2	-5.0

Characteristic	Symbol	Pin Under Test	MC1648 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	8	–	–	–	36	–	–	mAdc	–	–	7, 8	–	1, 14
Logic "1" Output Voltage	V_{OH}	3	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	–	12	7, 8	3	1, 14
Logic "0" Output Voltage	V_{OL}	3	-1.870	-1.635	-1.850	-1.620	-1.830	-1.595	Vdc	12	–	7, 8	3	1, 14
Bias Voltage	V_{Bias}*	10	-3.750	-3.400	-3.800	-3.500	-3.900	-3.600	Vdc	–	–	7, 8	–	1, 14
			Min	Typ Max	Min	Typ Max	Min	Typ Max						
Peak-to-Peak Tank Voltage	V_{p-p}	12	–	– –	–	500 –	–	– –	mV	See Figure 3	–	7, 8	3	1, 14
Output Duty Cycle	V_{DC}	3	–	– –	–	50 –	–	– –	%	See Figure 3	–	7, 8	3	1, 14
Oscillation Frequency	f_{max}	–	–	– –	195	225 –	–	– –	MHz	See Figure 3	–	7, 8	3	1, 14

*This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor tuning diode at this point.

FIGURE 3 – TEST CIRCUIT AND WAVEFORMS



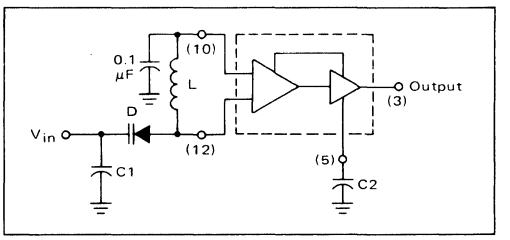
OPERATING CHARACTERISTICS

Figure 1 illustrates the circuit schematic for the MC1648. The oscillator incorporates positive feedback by coupling the base of transistor Q7 to the collector of Q8. An automatic gain control (AGC) is incorporated to limit the current through the emitter-coupled pair of transistors (Q7 and Q8) and allow optimum frequency response of the oscillator.

In order to maintain the high Q of the oscillator, and provide high spectral purity at the output, a cascode transistor (Q4) is used to translate from the emitter follower (Q5) to the output differential pair Q2 and Q3. Q2 and Q3, in conjunction with output transistor Q1, provide a highly buffered output which produces a square wave. Transistors Q10 thru Q14 provide the bias drive for the oscillator and output buffer. Figure 2 indicates the high spectral purity of the oscillator output (pin 3).

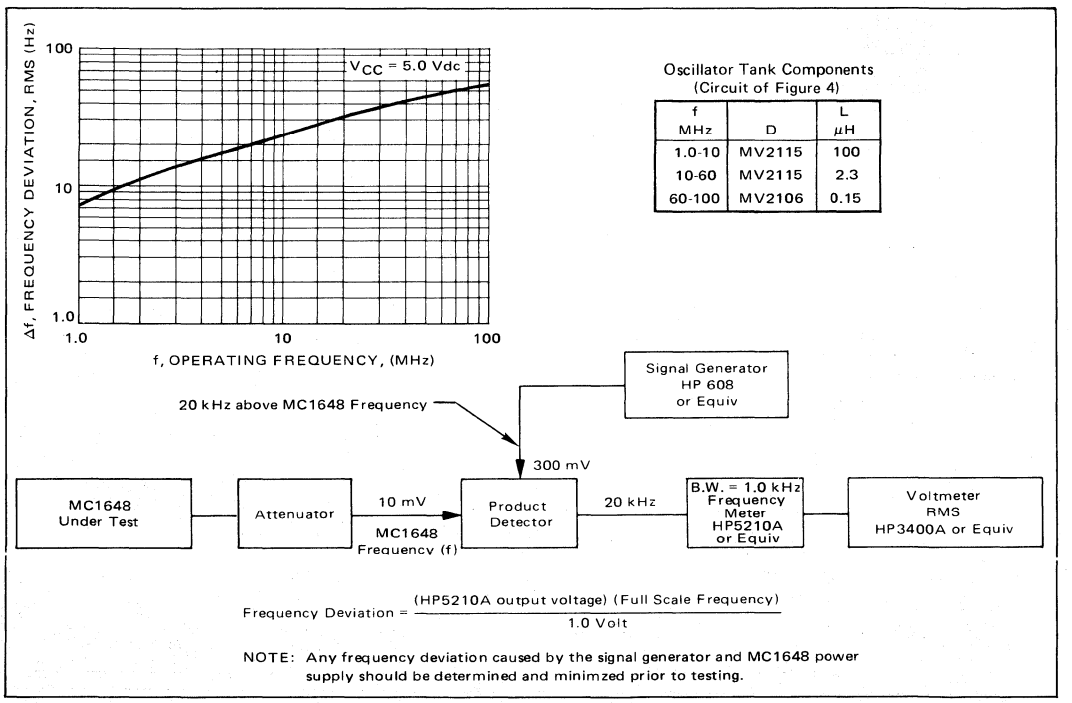
When operating the oscillator in the voltage controlled mode (Figure 4), it should be noted that the cathode of the varactor diode (D) should be biased at least 2 V_{BE} above V_{EE} ($\approx$ 1.4 V for positive supply operation).

FIGURE 4 – THE MC1648 OPERATING IN THE VOLTAGE CONTROLLED MODE



When the MC1648 is used with a constant dc voltage to the varactor diode, the output frequency will vary slightly because of internal noise. This variation is plotted versus operating frequency in Figure 5.

FIGURE 5 – NOISE DEVIATION TEST CIRCUIT AND WAVEFORM



Oscillator Tank Components
(Circuit of Figure 4)

f MHz	D	L μH
1.0-10	MV2115	100
10-60	MV2115	2.3
60-100	MV2106	0.15

$$\text{Frequency Deviation} = \frac{\text{(HP5210A output voltage) (Full Scale Frequency)}}{\text{1.0 Volt}}$$

NOTE: Any frequency deviation caused by the signal generator and MC1648 power supply should be determined and minimzed prior to testing.

TRANSFER CHARACTERISTICS IN THE VOLTAGE CONTROLLED MODE USING EXTERNAL VARACTOR DIODE AND COIL. $T_A = 25^oC$

FIGURE 6

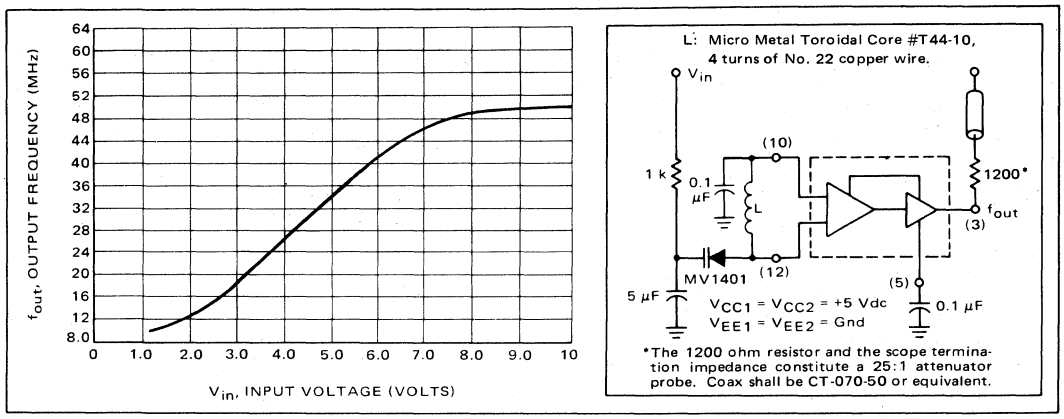


FIGURE 7

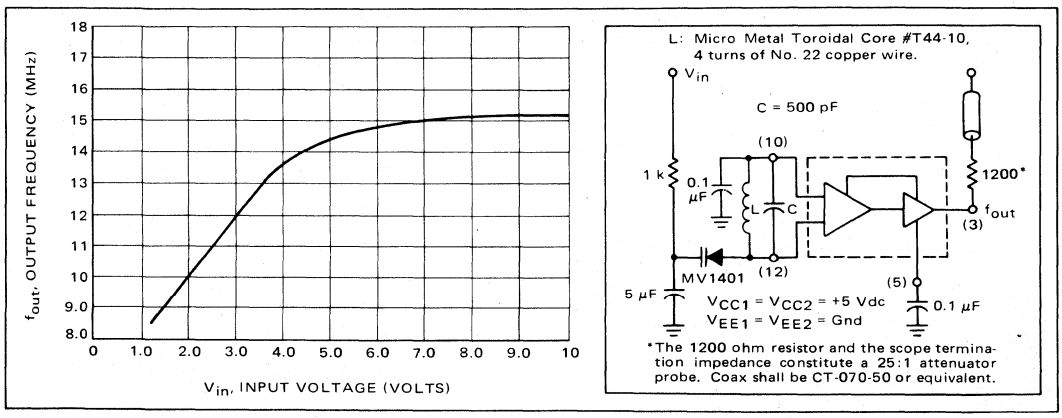
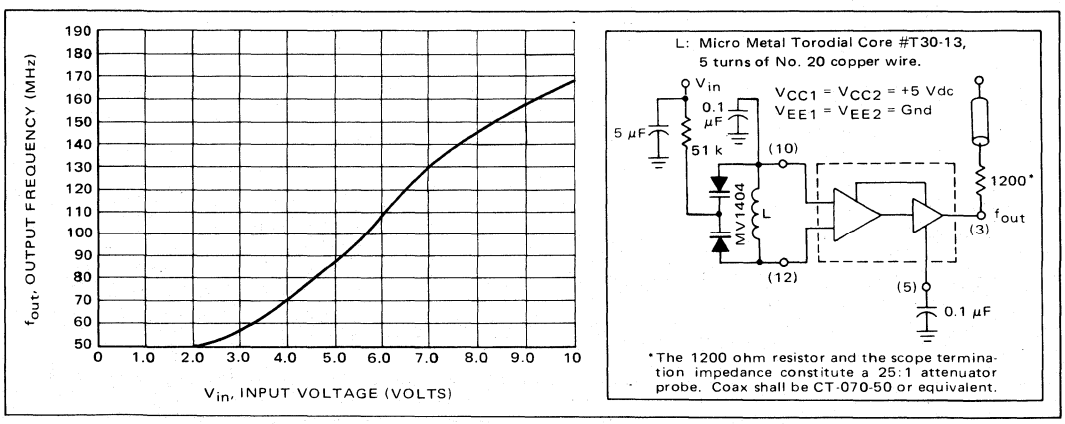


FIGURE 8



Typical transfer characteristics for the oscillator in the voltage controlled mode are shown in Figures 6, 7 and 8. Figures 6 and 8 show transfer characteristics employing only the capacitance of the varactor diode (pluse the input capacitance of the oscillator, 6 pF typical). Figure 7 illustrates the oscillator operating in a voltage controlled mode with the output frequency range limited. This is achieved by adding a capacitor in parallel with the tank circuit as shown. The 1 kΩ resistor in Figures 6 and 7 is used to protect the varactor diode during testing. It is not necessary as long as the dc input voltage does not cause the diode to become forward biased. The larger-valued resistor (51 kΩ) in Figure 8 is required to provide isolation for the high-impedance junctions of the two varactor diodes.

The tuning range of the oscillator in the voltage controlled mode may be calculated as:

$$\frac{f_{max}}{f_{min}} = \frac{\sqrt{C_D\ (max) + C_S}}{\sqrt{C_D\ (min) + C_S}}$$

where $f_{min} = \dfrac{1}{2\pi\sqrt{L\ (C_D\ (max) + C_S)}}$

C_S = shunt capacitance (input plus external capacitance).

C_D = varactor capacitance as a function of bias voltage.

Good RF and low-frequency bypassing is necessary on the power supply pins (see Figure 2).

Capacitors (C1 and C2 of Figure 4) should be used to bypass the AGC point and the VCO input (varactor diode), guaranteeing only dc levels at these points.

For output frequency operation between 1 MHz and 50 MHz a 0.1 μF capacitor is sufficient for C1 and C2. At higher frequencies, smaller values of capacitance should be used; at lower frequencies, larger values of capacitance. At higher frequencies the value of bypass capacitors depends directly upon the physical layout of the system. All bypassing should be as close to the package pins as possible to minimize unwanted lead inductance.

The peak-to-peak swing of the tank circuit is set internally by the AGC circuitry. Since voltage swing of the tank circuit provides the drive for the output buffer, the AGC potential directly affects the output waveform. If it is desired to have a sine wave at the output of the MC1648, a series resistor is tied from the AGC point to the most negative power potential (ground if +5.0 volt supply is used, -5.2 volts if a negative supply is used) as shown in Figure 10.

At frequencies above 100 MHz typ, it may be necessary to increase the tank circuit peak-to-peak voltage in order to maintain a square wave at the output of the MC1648. This is accomplished by tying a series resistor (1 kΩ minimum) from the AGC to the most positive power potential (+5.0 volts if a +5.0 volt supply is used, ground if a -5.2 volt supply is used). Figure 11 illustrates this principle.

3

APPLICATIONS INFORMATION

The phase locked loop shown in Figure 9 illustrates the use of the MC1648 as a voltage controlled oscillator. The figure illustrates a frequency synthesizer useful in tuners for FM broadcast, general aviation, maritime and land-mobile communications, amateur and CB receivers. The system operates from a single +5.0 Vdc supply, and requires no internal translation, since all components are compatible.

Frequency generation of this type offers the advantages of single crystal operation, simple channel selection, and elimination of special circuitry to prevent harmonic lock-up. Additional features include dc digital switching (preferable over RF switching with a multiple crystal system), and a broad range of tuning (up to 150 MHz, the range being set by the varactor diode).

The output frequency of the synthesizer loop is determined by the reference frequency and the number programmed at the programmable counter; $f_{out} = Nf_{ref}$. The channel spacing is equal to frequency (f_{ref}).

For additional information on applications and designs for phase locked-loops and digital frequency synthesizers, see Motorola Application Notes AN-532A, AN-535, AN-553, AN-564, and AN-594.

FIGURE 9 – TYPICAL FREQUENCY SYNTHESIZER APPLICATION

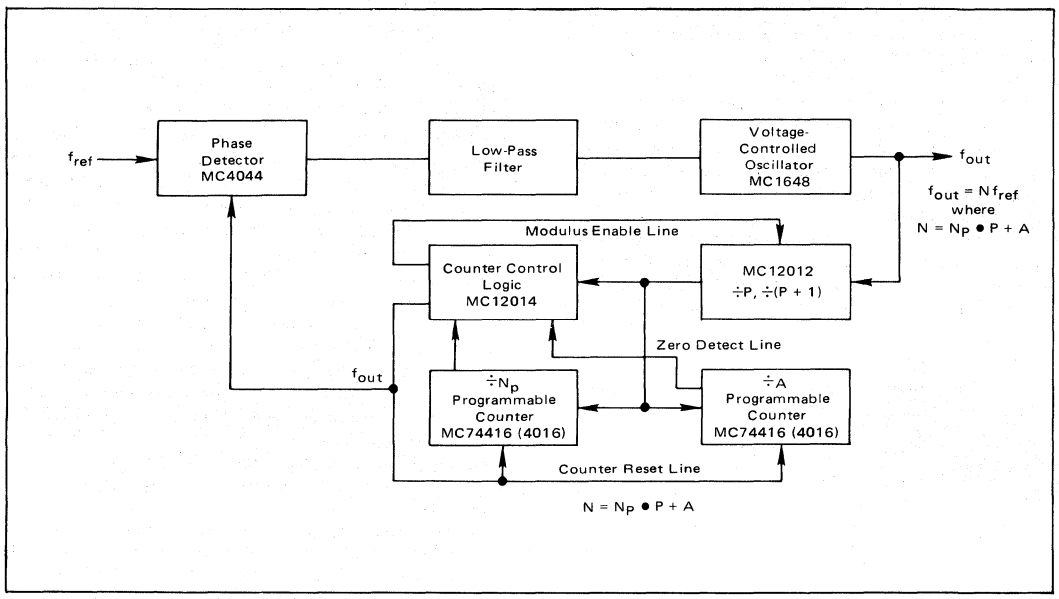


Figure 10 shows the MC1648 in the variable frequency mode operating from a +5.0 Vdc supply. To obtain a sine wave at the output, a resistor is added from the AGC circuit (pin 5) to V_{EE}.

Figure 11 shows the MC1648 in the variable frequency mode operating from a +5.0 Vdc supply. To extend the useful range of the device (maintain a square wave output above 175 MHz), a resistor is added to the AGC circuit at pin 5 (1 k-ohm minimum).

Figure 12 shows the MC1648 operating from +5.0 Vdc and +9.0 Vdc power supplies. This permits a higher voltage swing and higher output power than is possible from the MECL output (pin 3). Plots of output power versus total collector load resistance at pin 1 are given in Figures 13 and 14 for 100 MHz and 10 MHz operation. The total collector load includes R in parallel with Rp of L1 and C1 at resonance. The optimum value for R at 100 MHz is approximately 850 ohms.

FIGURE 10 – METHOD OF OBTAINING A SINE-WAVE OUTPUT

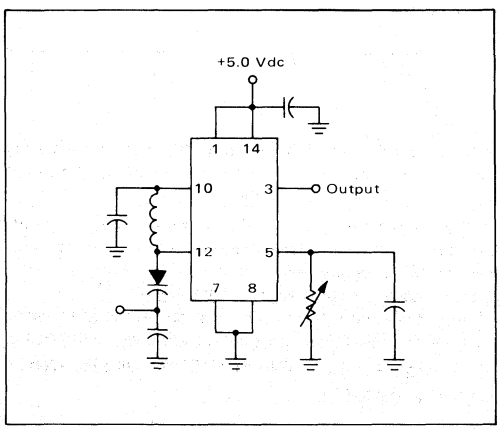


FIGURE 11 – METHOD OF EXTENDING THE USEFUL RANGE OF THE MC1648 (SQUARE WAVE OUTPUT)

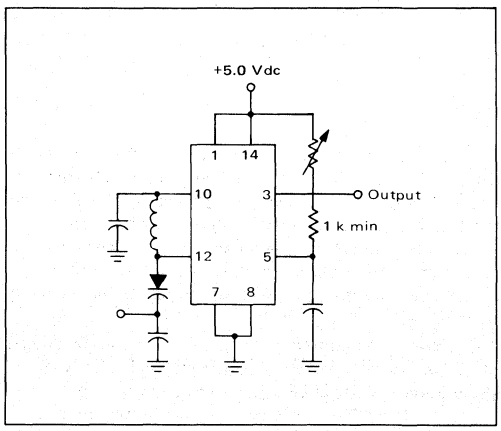


FIGURE 12 – CIRCUIT SCHEMATIC USED FOR COLLECTOR OUTPUT OPERATION

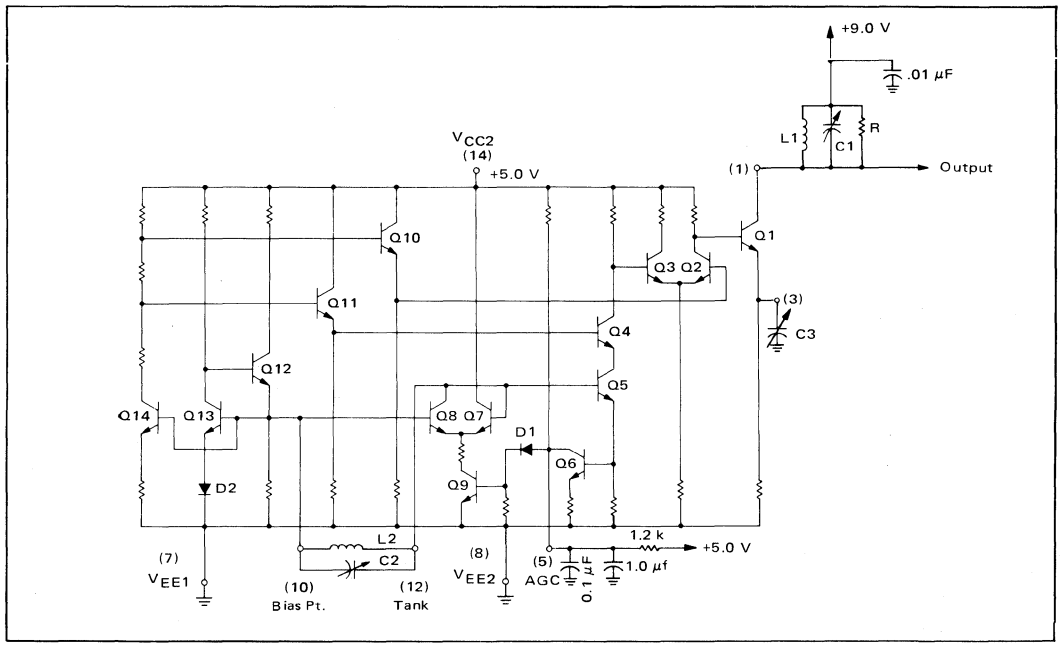


FIGURE 13 – POWER OUTPUT versus COLLECTOR LOAD

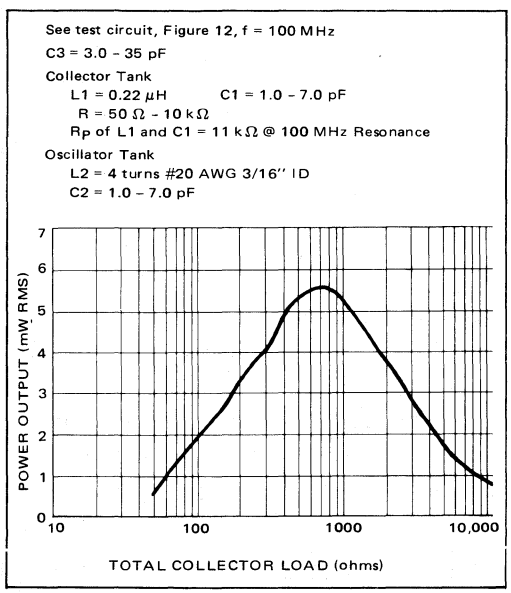
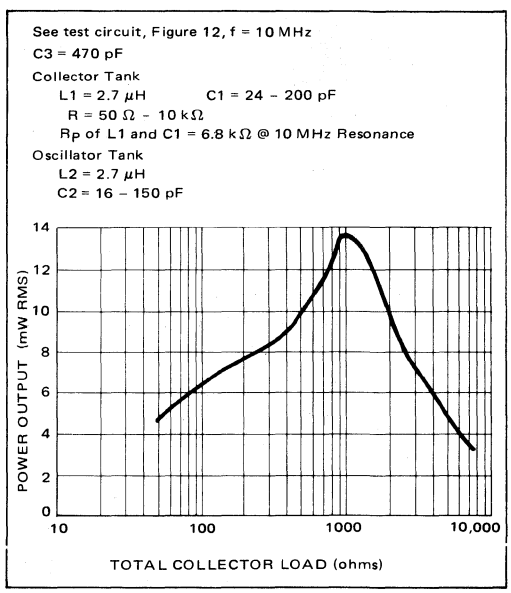


FIGURE 14 – POWER OUTPUT versus COLLECTOR LOAD



DUAL
VOLTAGE-CONTROLLED
MULTIVIBRATOR

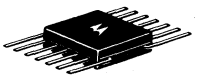
MC4324 • MC4024

The MC4324/4024 consists of two independent voltage-controlled multivibrators with output buffers. Variation of the output frequency over a 3.5-to-1 range is guaranteed with an input dc control voltage of 1.0 to 5.0 voltage.

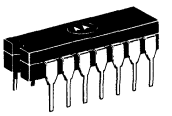
Operating frequency is specified at 25 MHz at 25°C. Operation to 15 MHz is possible over the specified temperature range. For higher frequency requirements, see the MC1648 (200 MHz) or the MC1658 (125 MHz) data sheet.

This device was designed specifically for use in phase-locked loops for digital frequency control. It can also be used in other applications requiring a voltage-controlled frequency, or as a stable fixed frequency oscillator (3.0 MHz to 15 MHz) by replacing the external control capacitor with a crystal.

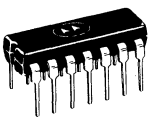
- Maximum Operating Frequency = 25 MHz Guaranteed @ 25°C
- Power Dissipation = 150 mW typ/pkg
- Output Loading Factor = 7



F SUFFIX
CERAMIC PACKAGE
CASE 607



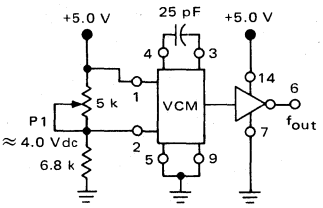
L SUFFIX
CERAMIC PACKAGE
CASE 632
(TO-116)



P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC4024 only)

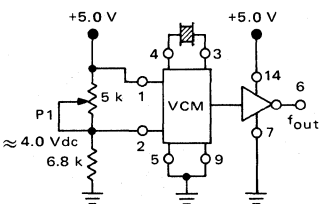
TYPICAL APPLICATIONS

FIGURE 1 – ASTABLE MULTIVIBRATOR



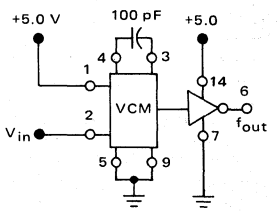
f_{out} = 10 MHz

FIGURE 2 – CRYSTAL CONTROLLED MULTIVIBRATOR



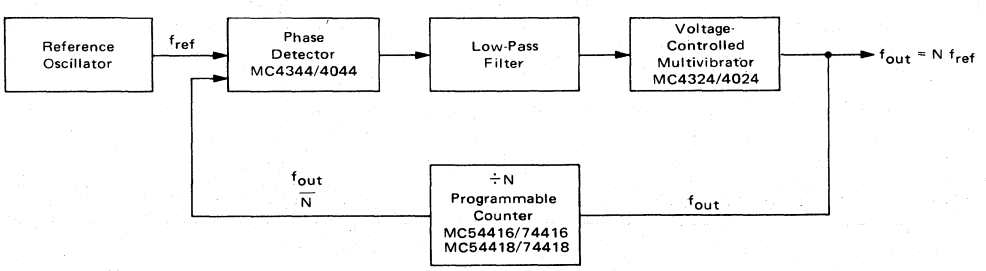
Crystal frequency can be pulled slightly by adjusting P1.

FIGURE 3 – VOLTAGE-CONTROLLED MULTIVIBRATOR

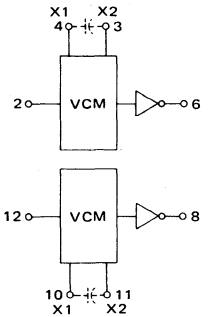


V_{in} = 2.5 V to 5.5 V
f_{out} = 1.0 MHz min, 5.0 MHz max

FIGURE 4 – PHASE-LOCKED, FREQUENCY SYNTHESIZER LOOP



ELECTRICAL CHARACTERISTICS

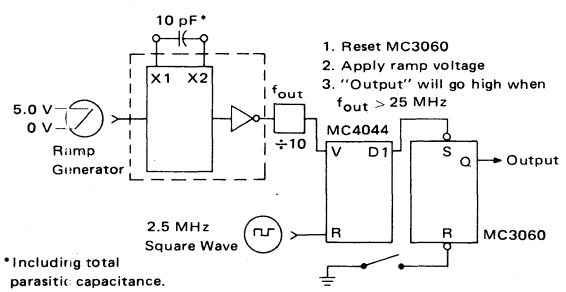


V_{CC}: VCM = 1, 13
Output Buffer = 14
Gnd: VCM = 5, 9
Output Buffer = 7
External Capacitor for Frequency Range Determination

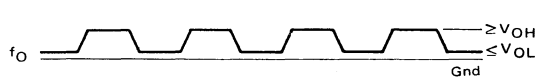
	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES mA I_{OL1}	I_{OL2}	I_{OH}	Volts V_{IH}	V_{CC}	V_{CCL}	V_{CCH}
MC4324	-55°C	9.8	11.2	-1.6	5.0	5.0	4.5	5.5
	+25°C	9.8	11.2	-1.6	5.0	5.0	4.5	5.5
	+125°C	9.8	11.2	-1.6	5.0	5.0	4.5	5.5
MC4024	0°C	9.8	11.2	-1.6	5.0	5.0	4.75	5.25
	+25°C	9.8	11.2	-1.6	5.0	5.0	4.75	5.25
	+75°C	9.8	11.2	-1.6	5.0	5.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC4324 Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC4024 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OH}	V_{IH}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																							
Forward Current	I_{in}	2	–	100	–	100	–	100	–	100	–	100	–	100	µAdc	–	–	–	2	–	–	14	5,7,9
		12	–	100	–	100	–	100	–	100	–	100	–	100	µAdc	–	–	–	12	–	–	14	5,7,9
Output																							
Output Voltage	V_{OL}	6	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	6	–	–	2	–	1,4,14	–	5,7,9
		8	–	↓	–	↓	–	↓	–	↓	–	↓	–	↓	↓	8	–	–	12	–	10,13,14	–	
		6	–		–		–		–		–		–			–	6	–	2	–	–	1,4,14	
		8	–		–		–		–		–		–			–	8	–	12	–	–	10,13,14	
	V_{OH}	6	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	–	6	2	–	1,3,14	–	5,7,9
		8	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	–	8	12	–	11,13,14	–	5,7,9
Short-Circuit Current	I_{OS}	6	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	mAdc	–	–	–	2	1,3,14	–	–	5,6,7,9
		8	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	mAdc	–	–	–	12	11,13,14	–	–	5,7,8,9
Power Requirements (Total Device)																							
Power Supply Drain	I_{CC}	1,3,14	–	–	–	37	–	–	–	–	–	37	–	–	mAdc	–	–	–	2,4,10,12	1,13,14	–	–	5,7,9

FIGURE 5 – AC TEST CIRCUIT AND WAVEFORMS



1. Reset MC3060
2. Apply ramp voltage
3. "Output" will go high when $f_{out} > 25$ MHz



(V_{CC} = 5.0 Vdc, T_A = 25°C)

TEST	SYMBOL	CONDITIONS	VALUE Min	VALUE Typ
Maximum Operating Frequency	f_{max}	C_X = 10 pF, V_{in} = 5.0 Vdc Frequency Ratio = 3.5:1	25 MHz	30 MHz
Ratio of Frequency of Oscillation Over Specified Input Voltage Range	$\frac{f_{high}}{f_{low}}$	C_X = 100 pF, V_{in} high = 5.0 Vdc, V_{in} low = 1.0 Vdc	3.5:1.0	4.5:1.0

MAXIMUM RATINGS

Rating		Value	Unit
Supply Operating Voltage Range	MC4324 MC4024	4.5 to 5.5 4.75 to 5.25	Vdc
Supply Voltage		+7.0	Vdc
Input Voltage		+5.5	Vdc
Output Voltage		+5.5	Vdc
Operating Temperature Range	MC4324 MC4024	-55 to +125 0 to +75	°C
Storage Temperature Range – Ceramic Package Plastic Package		-65 to +150 -55 to +125	°C
Maximum Junction Temperature	MC4324 MC4024	+175 +150	°C
Thermal Resistance - Junction To Case (θ_{JC}) Flat Ceramic Package Dual In-Line Ceramic Package Plastic Package		 0.06 0.05 0.07	°C/mW
Thermal Resistance - Junction To Ambient (θ_{JA}) Flat Ceramic Package Dual In-Line Ceramic Package Plastic Package		 0.21 0.15 0.15	°C/mW

FIGURE 6 – CIRCUIT SCHEMATIC

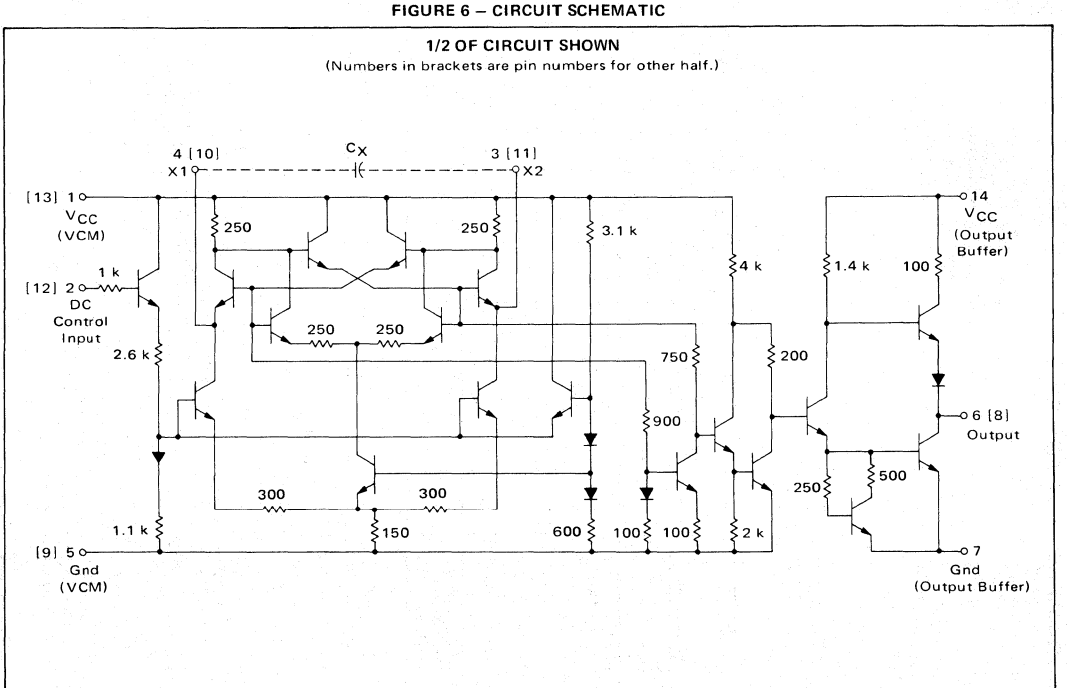


FIGURE 7 – FREQUENCY-CAPACITANCE PRODUCT

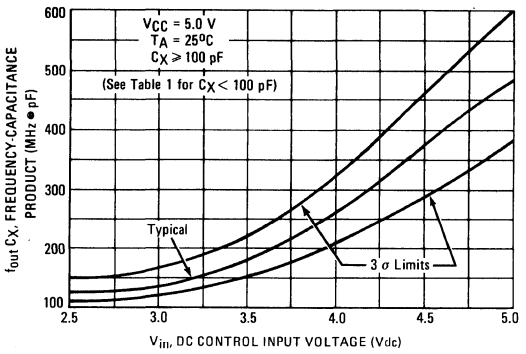


FIGURE 8 – FREQUENCY-VOLTAGE GAIN CHARACTERISTICS

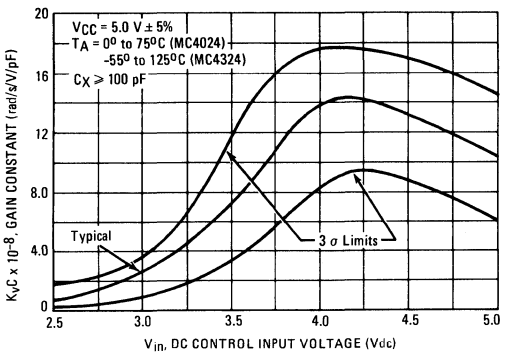


FIGURE 9 – TYPICAL FREQUENCY DEVIATION versus SUPPLY VOLTAGE

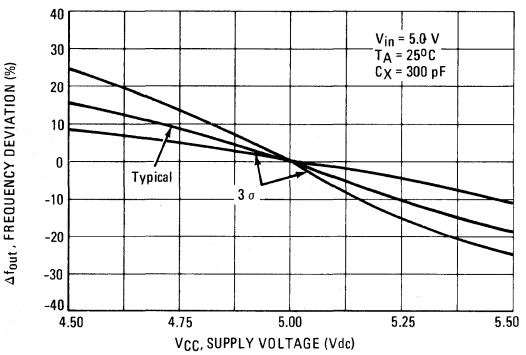


FIGURE 10 – TYPICAL FREQUENCY DEVIATION versus SUPPLY VOLTAGE

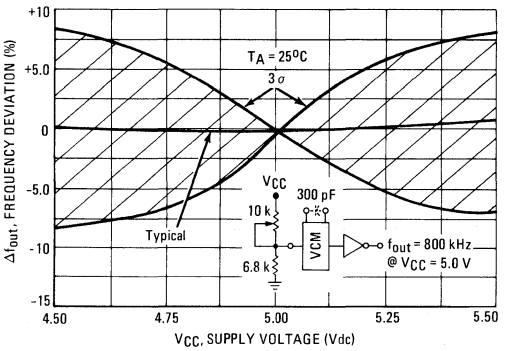


FIGURE 11 – FREQUENCY DEVIATION versus AMBIENT TEMPERATURE

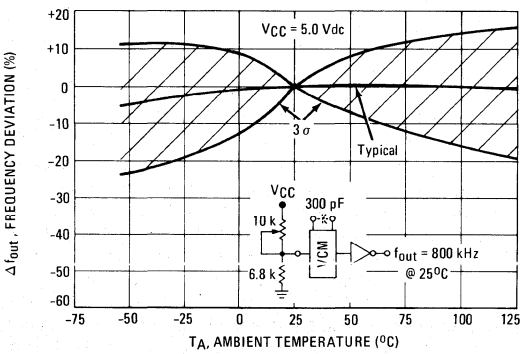
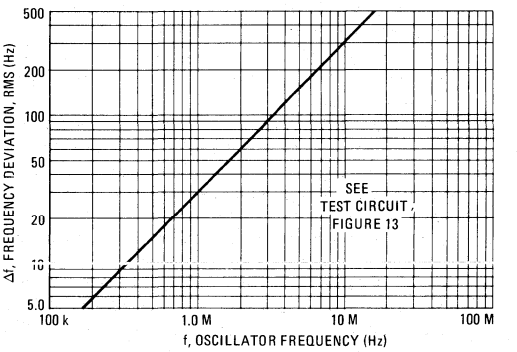
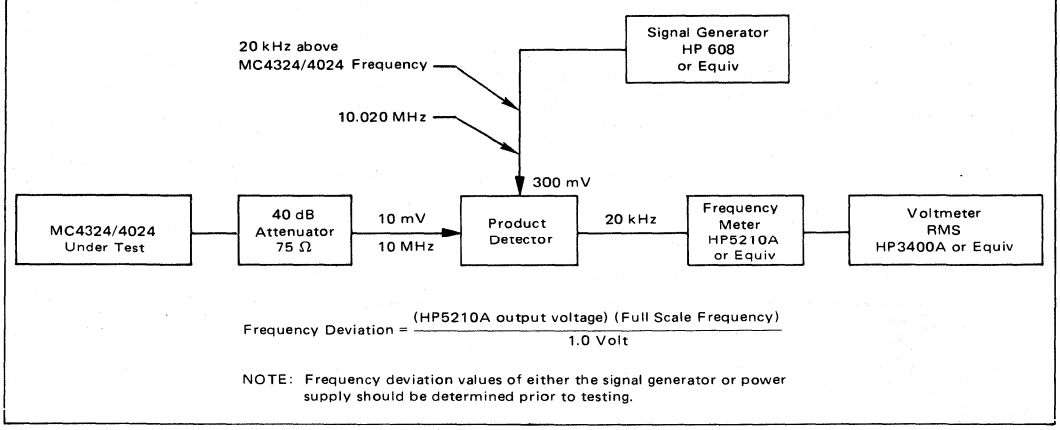


FIGURE 12 – RMS NOISE DEVIATION versus OSCILLATOR FREQUENCY



NOTE: Curves labeled as 3 σ limits denote that 99.7% of the devices tested fell within these limits.

FIGURE 13 – NOISE DEVIATION TEST CIRCUIT



$$\text{Frequency Deviation} = \frac{\text{(HP5210A output voltage) (Full Scale Frequency)}}{\text{1.0 Volt}}$$

NOTE: Frequency deviation values of either the signal generator or power supply should be determined prior to testing.

3

APPLICATIONS INFORMATION

Suggested Design Practices

Three power supply and three ground connections are provided in this circuit (each multivibrator has separate power supply and ground connections, and the output buffers have common power supply and ground pins). This provides isolation between VCM's and minimizes the effect of output buffer transients on the multivibrators in critical applications. The separation of power supply and ground lines also provides the capability of disabling one VCM by disconnecting its V_{CC} pin. However, all ground lines must always be connected to insure substrate grounding and proper isolation.

General design rules are:

1. Ground pins 5, 7, and 9 for all applications, including those where only one VCM is used.
2. Use capacitors with less than 50 nA leakage at plus and minus 3.0 volts. Capacitance values of 15 pF or greater are acceptable.
3. When operated in the free running mode, the minimum voltage applied to the DC Control input should be 60% of V_{CC} for good stability. The maximum voltage at this input should be V_{CC} + 0.5 volt.
4. When used in a phase-locked loop, the filter design should have a minimum DC Control input voltage of 1.0 volt and a maximum voltage of V_{CC} + 0.5 volt. The maximum restriction may be waived if the output impedance of the driving device is such that it will not source more than 10 mA at a voltage of V_{CC} + 0.5 volt.
5. The power supply for this device should be bypassed with a good quality RF-type capacitor of 500 to 1000 pF. Bypass capacitor lead lengths should be kept as short as possible. For best results, power supply voltage should be maintained as close to +5.0 V as possible. Under no conditions should the design require operation with a power supply voltage outside the range of 5.0 volts ± 10%.

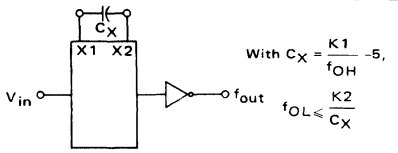
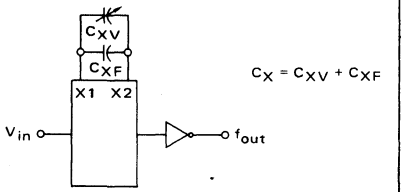
External Control Capacitor (C_X) Determination (See Table 1)

The operating frequency range of this multivibrator is controlled by the value of an external capacitor that is connected between X1 and X2. A tuning ratio of 3.5-to-1 and a maximum frequency of 25 MHz are guaranteed under ideal conditions (V_{CC} = 5.0 volts. T_A = 25°C). Under actual operating conditions, variations in supply voltage, ambient temperature, and internal component tolerances limit the tuning ratio (see Figures 7 thru 12). An improvement in tuning ratio can be achieved by providing a variable tuning capacitor to facilitate initial alignment of the circuit.

Figures 7 through 11 show typical and suggested design limit information for important VCM characteristics. The suggested design limits are based on operation over the specified temperature range with a supply voltage of 5.0 volts ±5% unless otherwise noted. They include a safety factor of three times the estimated standard deviation.

Figures 7 and 8 provide data for any external control capacitor value greater than 100 pF. With smaller capacitor values, the curves are effectively moved downward. For example, a typical curve of frequency versus control voltage would be very nearly identical to the lower suggested

TABLE 1 – EXTERNAL CONTROL CAPACITOR VALUE DETERMINATION

CONFIGURATION	T_A	V_{CC}	VALUES OF K				
			K1	K2	K3	K4	K5
 With $C_X = \frac{K1}{f_{OH}} - 5$, $f_{OL} \leq \frac{K2}{C_X}$	25°C ±3°C	5.0 V	385	150	600	110	1.0
		5.0 V ±5%	325	175	680	125	1.14
		5.0 V ±10%	290	190	750	140	1.25
 $C_X = C_{XV} + C_{XF}$	0°C to 75°C	5.0 V	335	165	660	120	1.10
		5.0 V ±5%	280	190	750	140	1.25
		5.0 V ±10%	250	200	840	150	1.40
Choose C_{XF} and C_{XV} such that C_X can be adjusted to: $\frac{K1}{f_{OH}} - 5 \leq C_X \leq \frac{K3}{f_{OH}} - 5$ With $V_{in} = V_{CC} = 5.0$ V, adjust C_X to obtain: $f_{out} = K5\ (f_{OH})$ Then: $f_{OL} \leq \frac{K4}{K1} f_{OH}$	-55°C to 125°C	5.0 V	300	175	690	125	1.15
		5.0 V ±5%	260	200	780	145	1.30
		5.0 V ±10%	230	210	860	155	1.45

Definitions: f_{OH} = Output frequency with $V_{in} = V_{CC}$
f_{OL} = Output frequency with V_{in} = 2.5 V
(Frequencies in MHz, C_X in pF)

design limit of Figure 7 if a 15 pF capacitor is used. To use Figure 7, divide on the ordinate by the capacitor value in picofarads to obtain output frequency in megahertz. In Figure 8, the ordinate axis is multiplied by the capacitor value in picofarads to obtain the gain constant (K_V) in radians/second/volt.

Frequency Stability

When the MC4324/4024 is used as a fixed-frequency oscillator (V_{in} constant), the output frequency will vary slightly because of internal noise. This variation is indicated by Figure 12 for the circuit of Figure 13. These variations are relatively independent (< 10%) of changes in temperature and supply voltage.

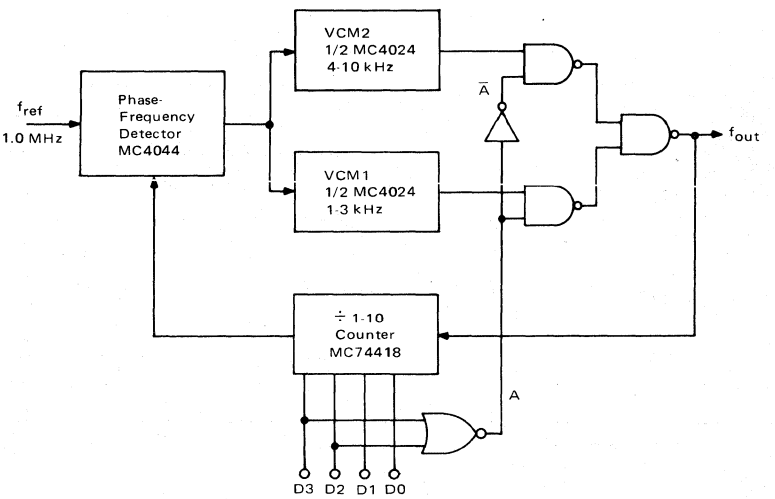
10-to-1 Frequency Synthesizer

A frequency synthesizer covering a 10-to-1 range is shown in Figure 14. Three packages are required to complete the loop: The MC4344/4044 phase-frequency detector, the MC4324/4024 dual voltage-controlled multivibrator, and the MC54418/74418 programmable counter. Two VCM's (one package) are used to obtain the required frequency range. Each VCM is capable of operating over a 3-to-1 range, thus VCM1 is used for the lower portion of the times ten range and VCM2 covers the upper end. The proper divide ratio is set into the programmable counter and the VCM for that frequency is selected by control gates. The other VCM is left to be free running since its output is gated out of the feedback path.

Normally with a single VCM the loop gain would vary over a 10-to-1 range due to the range of the counter ratios. This affects the bandwidth, lockup time, and damping ratio severely. Utilizing two VCM's reduces this change in loop gain from 10-to-1 to 3-to-1 as a result of the different sensitivities of the two VCM's due to the different frequency ranges. This change of VCM sensitivity (3-to-1) is of such a direction to compensate for loop gain variations due to the programmable counter.

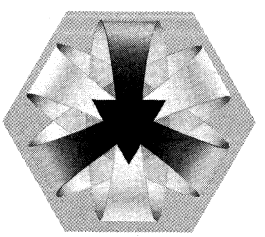
The overall concept of multi-VCM operation can be expanded for ranges greater than 10-to-1. Four VCM's (two packages) could be used to cover a 100-to-1 range.

FIGURE 14 – 10-TO-1 FREQUENCY SYNTHESIZER



÷N	Input D3	D2	D1	D0	A	VCM1 kHz	VCM2 kHz	f_{out} kHz
1	0	0	0	1	1	1	X	1
2	0	0	1	0	1	2	X	2
3	0	0	1	1	1	3	X	3
4	0	1	0	0	0	X	4	4
5	0	1	0	1	0	X	5	5
6	0	1	1	0	0	X	6	6
7	0	1	1	1	0	X	7	7
8	1	0	0	0	0	X	8	8
9	1	0	0	1	0	X	9	9
10	1	0	1	0	0	X	10	10

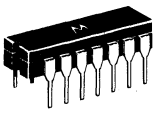
MIXERS



DIGITAL MIXER/TRANSLATOR
(D Flip-Flop w/Translator)

The MC12000 is intended for use as a digital mixer in phase-locked loop frequency synthesizers and other applications where a MECL "D" flip-flop with translators is required. Toggle frequency is typically 250 MHz. MTTL to MECL and MECL to MTTL translators are provided to facilitate interfacing with MECL or MTTL circuits.

The MC12000 is designed to operate from a single power supply of either +5.0 Vdc or -5.2 Vdc.



CERAMIC PACKAGE
CASE 632

Pin Assignment

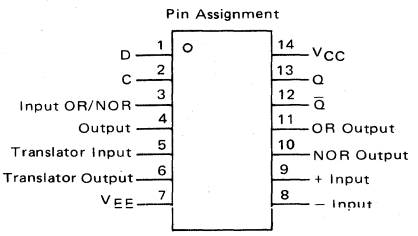
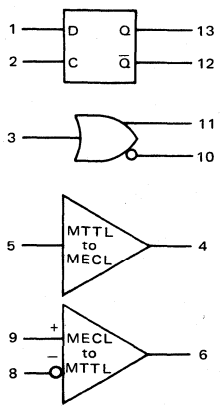


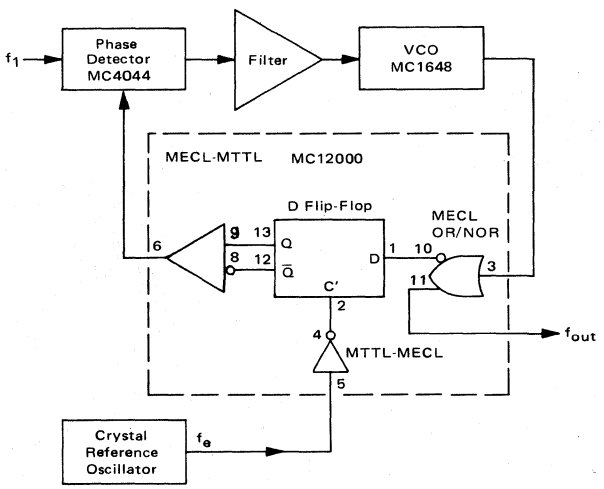
FIGURE 1 – LOGIC DIAGRAM



V_{CC} = Pin 14
V_{EE} = Pin 7

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

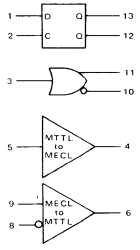
FIGURE 2 – TYPICAL DIGITAL MIXER



Note: All MECL outputs have 510-ohm internal pulldown resistors.

ELECTRICAL CHARACTERISTICS

Supply Voltage = +5.0 V



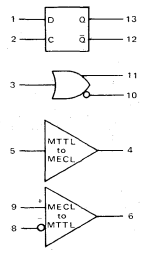
@ Test Temperature	TEST VOLTAGE/CURRENT VALUES: Volts V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IH}	V_{IHA}	V_R	V_{IHT}	V_{ILT}	V_{CC}	mA I_L	I_{OL}	I_{OH}
0°C	+4.160	+3.130	+3.855	+3.510	+0.5	+2.4	+5.0	+4.5	+2.0	+0.8	+5.0	-2.5	16	-1.6
25°C	+4.190	+3.150	+3.895	+3.525	+0.5	+2.4	+5.0	+4.5	+2.0	+0.8	+5.0	-2.5	16	-1.6
75°C	+4.280	+3.170	+3.955	+3.550	+0.5	+2.4	+5.0	+4.5	+2.0	+0.8	+5.0	-2.5	16	-1.6

Characteristic	Symbol	Pin Under Test	MC12000 0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{IHT}	V_{ILT}	V_{CC}	I_L	I_{OL}	I_{OH}	(V_{EE}) Gnd
Power Supply Drain Current	I_E	7	–	–	–	85	–	–	–	mAdc	–	–	–	–	–	–	–	–	–	–	14	–	–	–	7
Input Current	I_{INH1}	1	–	–	–	–	200	–	–	μAdc	1	2	–	–	–	–	–	–	–	–	14	–	–	–	7
		2	–	–	–	–	200	–	–		2	1	–	–	–	–	–	–	–	–		–	–	–	
		3	–	–	–	–	200	–	–		3	–	–	–	–	–	–	–	–	–		–	–	–	
	I_{INH2}	5	–	4.0	–	–	40	–	40		–	–	–	–	–	–	5	–	–	–		–	–	–	
	I_{INH3}	8	–	–	3.8	–	6.5	–	–	mAdc	9	8	–	–	–	–	–	–	–	–		–	–	–	
		9	–	–	3.8	–	6.5	–	–		9	8	–	–	–	–	–	–	–	–		–	–	–	
	I_{INL1} (Leakage Current)	1	–	–	–	–	2.0	–	–	μAdc	–	–	–	–	–	–	–	–	–	–	14	–	–	–	1,7
		2	–	–	–	–	2.0	–	–		–	–	–	–	–	–	–	–	–	–		–	–	–	2,7
		3	–	–	–	–	2.0	–	–		–	–	–	–	–	–	–	–	–	–		–	–	–	3,7
	I_{INL2}	5	–	-1.6	–	–	-1.6	–	-1.6	mAdc	–	–	–	–	5	–	–	–	–	–		–	–	–	7
	I_{INL3}	8	–	–	3.8	–	6.5	–	–		8	9	–	–	–	–	–	–	–	–		–	–	–	
		9	–	–	2.0	–	4.0	–	–		8	9	–	–	–	–	–	–	–	–		–	–	–	
Logic "1" Output Voltage	V_{OH1}	4	4.000	4.160	4.040	–	4.190	4.100	4.280	Vdc	–	–	–	–	–	5	–	–	–	–	14	4	–	–	7
		10				–						3										10	–	–	
		11				–					3	–										11	–	–	
		12†				–					–	1										12	–	–	
		13†				–					1	–										13	–	–	
	V_{OH2}	6	2.400	–	2.400	–	–	2.400	–	Vdc	9	8	–	–	–	–	–	–	–	–	14	–	–	6	7
Logic "0" Output Voltage	V_{OL1}	4	3.130	3.370	3.150	–	3.380	3.170	3.410	Vdc	–	–	–	–	5	–	–	–	–	–	14	4	–	–	7
		10				–					3	–			–							10	–	–	
		11				–					–	3			–							11	–	–	
		12†				–					1	–			–							12	–	–	
		13†				–					–	1			–							13	–	–	
	V_{OL2}	6	–	0.500	–	–	0.500	–	0.500	Vdc	8	9	–	–	–	–	–	–	–	–	14	–	6	–	7
Logic "1" Threshold Voltage	V_{OHA}	4	3.980	–	4.020	–	–	4.080	–	Vdc	–	–	–	–	–	–	–	–	5	–	14	4	–	–	7
		10		–		–	–		–		–	–	–	3	–	–	–	–	–	–		10	–	–	
		11		–		–	–		–		–	–	3	–	–	–	–	–	–	–		11	–	–	
		12†		–		–	–		–		–	–	–	1	–	–	–	–	–	–		12	–	–	
		13†		–		–	–		–		–	–	1	–	–	–	–	–	–	–		13	–	–	
Logic "0" Threshold Voltage	V_{OLA}	4	–	3.390	–	–	3.400	–	3.430	Vdc	–	–	–	–	–	–	–	–	–	5	14	4	–	–	7
		10	–		–	–		–			–	–	3	–	–	–	–	–	–	–		10	–	–	
		11	–		–	–		–			–	–	–	3	–	–	–	–	–	–		11	–	–	
		12†	–		–	–		–			–	–	1	–	–	–	–	–	–	–		12	–	–	
		13†	–		–	–		–			–	–	–	1	–	–	–	–	–	–		13	–	–	
Short Circuit Current	I_{SC}	6	-20	-65	-20	–	-65	-20	-65	mAdc	9	8	–	–	–	–	–	–	–	–	14	–	–	–	6,7

†Output Level to be measured after a clock pulse has been applied to the C input (pin 2) V_{IHmax} / V_{ILmin}

ELECTRICAL CHARACTERISTICS

Supply Voltage = -5.2 V



@ Test Temperature	TEST VOLTAGE/CURRENT VALUES: Volts V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{IHT}	V_{ILT}	V_{EE}	mA I_L	I_{OL}	I_{OH}
0°C	-0.840	-1.870	-1.145	-1.490	-4.7	-2.8	+0.0	-0.7	-3.2	-4.4	-5.2	-2.5	16	-1.6
25°C	-0.810	-1.850	-1.105	-1.475	-4.7	-2.8	+0.0	-0.7	-3.2	-4.4	-5.2	-2.5	16	-1.6
75°C	-0.720	-1.830	-1.045	-1.450	-4.7	-2.8	+0.0	-0.7	-3.2	-4.4	-5.2	-2.5	16	-1.6

Characteristic	Symbol	Pin Under Test	MC12000 0°C Min	0°C Max	25°C Min	25°C Typ	25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{IHT}	V_{ILT}	V_{EE}	I_L	I_{OL}	I_{OL}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	7	–	–	–	90	–	–	–	mAdc	–	–	–	–	–	–	–	–	–	–	7	–	–	–	14
Input Current	I_{INH1}	1	–	–	–	–	200	–	–	µAdc	1	2	–	–	–	–	–	–	–	–	7	–	–	–	14
		2	–	–	–	–	200	–	–		2	1	–	–	–	–	–	–	–	–		–	–	–	
		3	–	–	–	–	200	–	–		3	–	–	–	–	–	–	–	–	–		–	–	–	
	I_{INH2}	5	–	40	–	–	40	–	40		–	–	–	–	–	–	5	–	–	–		–	–	–	
	I_{INH3}	8	–	–	3.8	–	6.5	–	–	mAdc	9	8	–	–	–	–	–	–	–	–		–	–	–	
		9	–	–	3.8	–	6.5	–	–		9	8	–	–	–	–	–	–	–	–		–	–	–	
	I_{INL1} (Leakage Current)	1	–	–	–	–	2.0	–	–	µAdc	–	–	–	–	–	–	–	–	–	–	1,7	–	–	–	14
		2	–	–	–	–	2.0	–	–		–	–	–	–	–	–	–	–	–	–	2,7	–	–	–	
		3	–	–	–	–	2.0	–	–		–	–	–	–	–	–	–	–	–	–	3,7	–	–	–	
	I_{INL2}	5	–	-1.6	–	–	-1.6	–	-1.6	mAdc	–	–	–	–	5	–	–	–	–	–	7	–	–	–	
	I_{INL3}	8	–	–	3.8	–	6.5	–	–		8	9	–	–	–	–	–	–	–	–		–	–	–	
		9	–	–	2.0	–	4.0	–	–		8	9	–	–	–	–	–	–	–	–		–	–	–	
Logic "1" Output Voltage	V_{OH1}	4	-1.000	-0.840	-0.960	–	-0.810	-0.900	-0.720	Vdc	–	–	–	–	–	5	–	–	–	–	7	4	–	–	14
		10				–					–	3	–	–	–	–	–	–	–	–		10	–	–	
		11				–					3	–	–	–	–	–	–	–	–	–		11	–	–	
		12†				–					–	1	–	–	–	–	–	–	–	–		12	–	–	
		13†				–					1	–	–	–	–	–	–	–	–	–		13	–	–	
	V_{OH2}	6	-2.800	–	-2.800	–	–	-2.800	–	Vdc	9	8	–	–	–	–	–	–	–	–	7	–	–	6	14
Logic "0" Output Voltage	V_{OL1}	4	-1.870	-1.635	-1.850	–	-1.620	-1.830	-1.595	Vdc	–	–	–	–	5	–	–	–	–	–	7	4	–	–	14
		10				–					3	–	–	–	–	–	–	–	–	–		10	–	–	
		11				–					–	3	–	–	–	–	–	–	–	–		11	–	–	
		12†				–					1	–	–	–	–	–	–	–	–	–		12	–	–	
		13†				–					–	1	–	–	–	–	–	–	–	–		13	–	–	
	V_{OL2}	6	–	-4.700	–	–	-4.700	–	-4.700	Vdc	8	9	–	–	–	–	–	–	–	–	7	–	6	–	14
Logic "1" Threshold Voltage	V_{OHA}	4	-1.020	–	-0.980	–	–	-0.920	–	Vdc	–	–	–	–	–	–	–	–	5	–	7	4	–	–	14
		10		–		–	–		–		–	–	–	3	–	–	–	–	–	–		10	–	–	
		11		–		–	–		–		–	–	3	–	–	–	–	–	–	–		11	–	–	
		12†		–		–	–		–		–	–	–	1	–	–	–	–	–	–		12	–	–	
		13†		–		–	–		–		–	–	1	–	–	–	–	–	–	–		13	–	–	
Logic "0" Threshold Voltage	V_{OLA}	4	–	-1.615	–	–	-1.600	–	-1.575	Vdc	–	–	–	–	–	–	–	–	–	5	7	4	–	–	14
		10	–		–	–		–			–	–	3	–	–	–	–	–	–	–		10	–	–	
		11	–		–	–		–			–	–	–	3	–	–	–	–	–	–		11	–	–	
		12†	–		–	–		–			–	–	1	–	–	–	–	–	–	–		12	–	–	
		13†	–		–	–		–			–	–	–	1	–	–	–	–	–	–		13	–	–	
Short Circuit Current	I_{SC}	6	-20	-65	-20	–	-65	-20	-65	mAdc	9	8	–	–	–	–	–	–	–	–	6,7	–	–	–	14

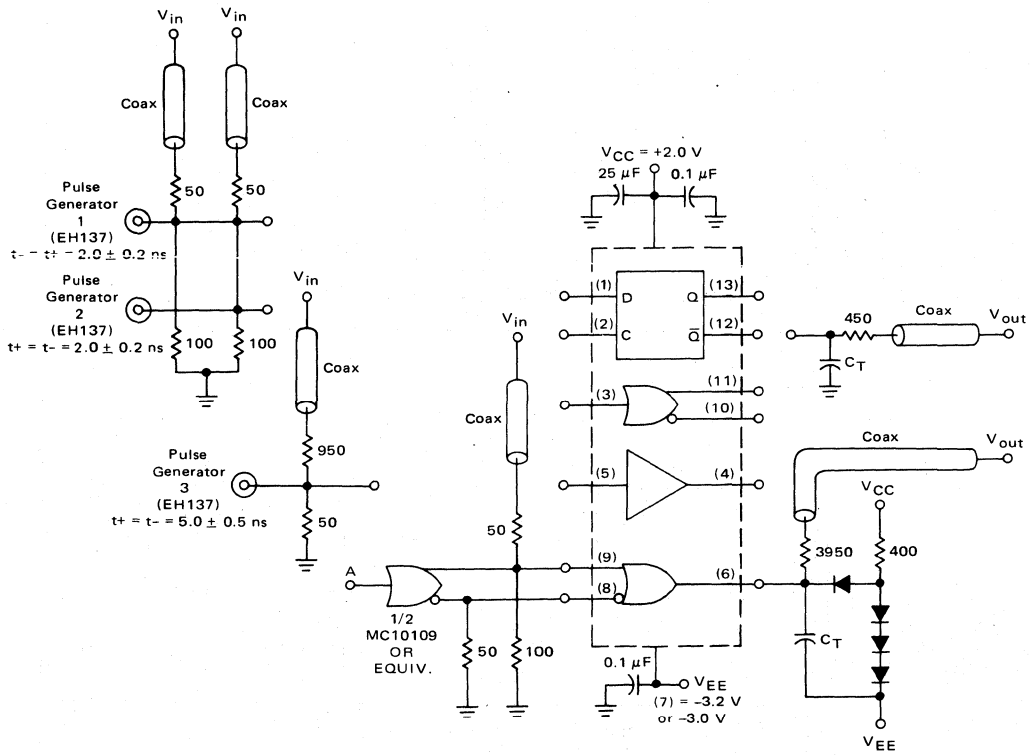
†Output Level to be measured after a clock pulse has been applied to the C input (pin 2) V_{IHmax} V_{ILmin}

AC ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC12000 0°C Min	MC12000 0°C Max	MC12000 +25°C Min	MC12000 +25°C Typ	MC12000 +25°C Max	MC12000 +75°C Min	MC12000 +75°C Max	Unit	TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW: Pulse Gen. 1	Pulse Gen. 2	Pulse Gen. 3	Pulse Out	V_{EE} -3.2 V or -3.0 V	V_{CC} +2.0 V
Propagation Delay (See Figure 4)	t_{2+13+}	2,13	–	–	1.5	2.4	4.0	–	–	ns	2	1	–	13	7	14
	t_{2+13-}	2,13	–	–	1.5	2.4	4.0	–	–	ns	2	1	–	13	7	14
	t_{2+12+}	2,12	–	–	1.5	2.4	4.0	–	–	ns	2	1	–	12	7	14
	t_{2+12-}	2,12	–	–	1.5	2.4	4.0	–	–	ns	2	1	–	12	7	14
	t_{3+11+}	3,11	–	–	1.0	1.5	3.0	–	–	ns	3	–	–	11	7	14
	t_{3-11-}	3,11	–	–	1.0	1.5	3.0	–	–	ns	3	–	–	11	7	14
	t_{3+10-}	3,10	–	–	1.0	1.5	3.0	–	–	ns	3	–	–	10	7	14
	t_{3-10+}	3,10	–	–	1.0	1.5	3.0	–	–	ns	3	–	–	10	7	14
	t_{5+4+}	5,4	–	–	2.0	3	5.0	–	–	ns	–	–	5	4	7	14
	t_{5-4-}	5,4	–	–	1.0	1.5	3.0	–	–	ns	–	–	5	4	7	14
	t_{9+6+}	9,6	–	–	4.0	8.0	12.0	–	–	ns	A	–	–	6	7	14
	t_{9-6-}	9,6	–	–	3.0	5.0	10.0	–	–	ns	A	–	–	6	7	14
Output Rise Time (See Figure 4)	t_{13+}	13	–	–	–	2.8	–	–	–	ns	2	1	–	13	7	14
	t_{12+}	12	–	–	–	2.8	–	–	–	ns	2	1	–	12	7	14
	t_{11+}	11	–	–	–	2.0	–	–	–	ns	3	–	–	11	7	14
	t_{10+}	10	–	–	–	2.0	–	–	–	ns	3	–	–	10	7	14
	t_{4+}	4	–	–	–	2.4	–	–	–	ns	–	–	5	4	7	14
Output Fall Time (See Figure 4)	t_{13-}	13	–	–	–	2.8	–	–	–	ns	2	1	–	13	7	14
	t_{12-}	12	–	–	–	2.8	–	–	–	ns	2	1	–	12	7	14
	t_{11-}	11	–	–	–	2.0	–	–	–	ns	3	–	–	11	7	14
	t_{10-}	10	–	–	–	2.0	–	–	–	ns	3	–	–	10	7	14
	t_{4-}	4	–	–	–	2.4	–	–	–	ns	–	–	5	4	7	14
Setup Time (See Figure 5)	$t_{setup"1"}$	13	–	–	–	0.2	–	–	–	ns	2	1	–	–	7	14
	$t_{setup"0"}$	13	–	–	–	0.7	–	–	–	ns	2	1	–	–	7	14
Hold Time (See Figure 5)	$t_{hold"1"}$	13	–	–	–	0.0	–	–	–	ns	2	1	–	–	7	14
	$t_{hold"0"}$	13	–	–	–	1.0	–	–	–	ns	2	1	–	–	7	14
Toggle Frequency (See Figure 6)	f_{tog}	13	–	–	–	250	–	–	–	MHz	–	–	–	–	7	14

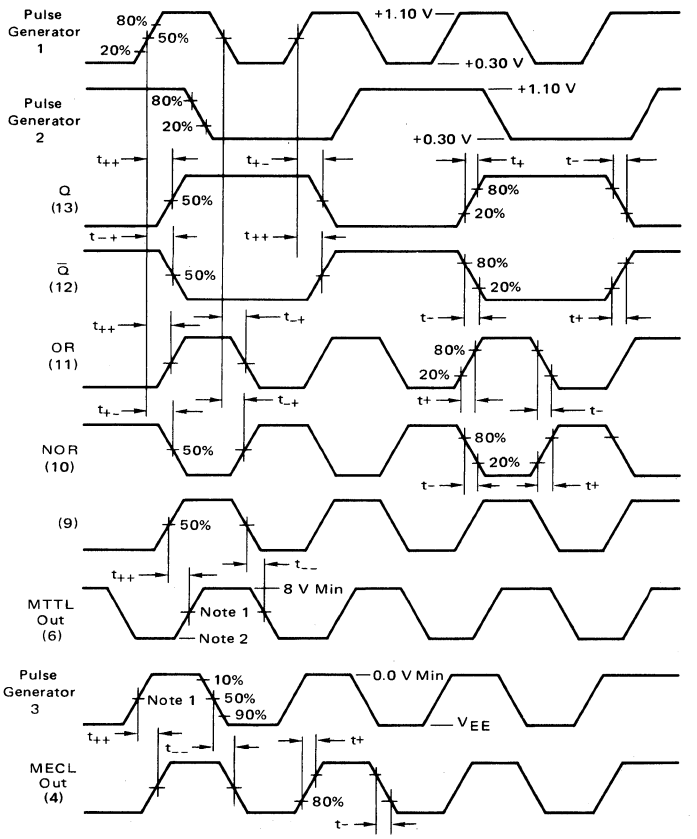
FIGURE 3 – SWITCHING TIME TEST CIRCUIT

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. All unused cables must be terminated with a 50 ohm resistor ± 1%.



C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

FIGURE 4 – AC TEST VOLTAGE WAVEFORMS



NOTES:
1. V_{EE} + 1.5 V
2. V_{EE} + 0.5 V max

FIGURE 5 – SETUP AND HOLD TIME WAVEFORMS (See Figure 3)

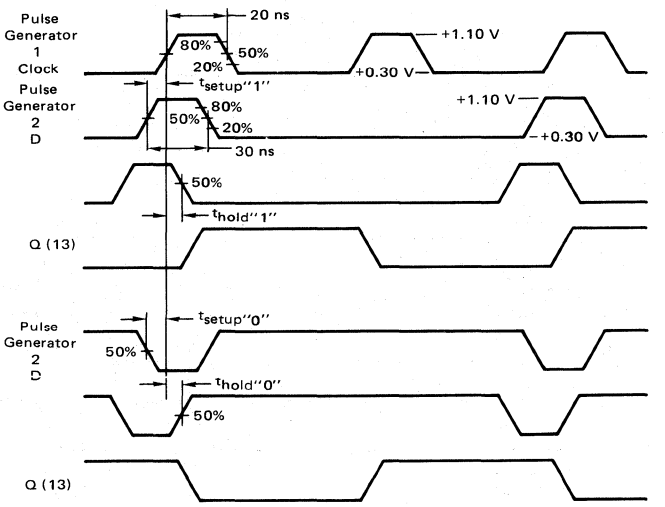
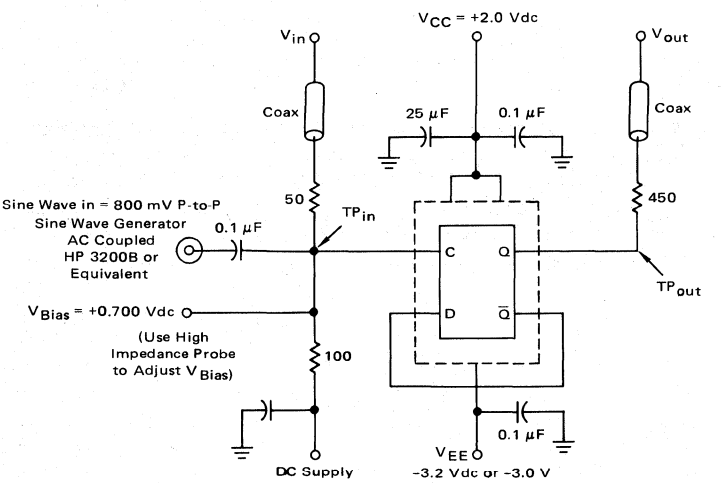


FIGURE 6 – TOGGLE FREQUENCY TEST CIRCUIT



The maximum Toggle Frequency of MC12000 has been exceeded when either:

1. The output Peak-to-Peak voltage swing falls below 600 mV

   or

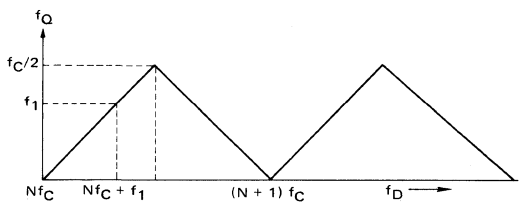
2. The devices cease to Toggle (divide by 2).

MC12000 DIGITAL MIXER

This device is a digital mixer designed to operate with logic levels at its input and output ports. In operation it is an MECL type "D" flip-flop with level translators to and from MTTL to accomodate most interfacing demands. Output frequency (f_Q) as a function of "D" and clock inputs is shown in Figure 7. It can be seen that either direct or harmonic mixing may be employed, that is, f_Q may be either the difference between f_D and f_C or the difference between f_D and the Nth harmonic of f_C.

One particular advantage of mixing in phase locked loops (PLL) is that lower frequencies may be generated for use in portions of the circuit where digital processing is done (with divide-by-P network and/or phase detector). Lower frequency operation often reduces overall system cost since a less expensive logic form may be utilized. However use of the mixing technique is not a panacea for all VHF applications and the design of such synthesizer systems must be approached with care.

FIGURE 7



Use of the MC12000 in a non-harmonic PLL is straightforward (Figure 8). Output frequency is the sum of both input quantities ($f_1 + f_C$) as long as f_1 is less than $f_C/2$ (See Figure 7), since f_Q can go no higher than that. Unless VCO output range is restricted somewhat there is a chance also that the loop may operate at the second harmonic of f_C. This problem is minimal in the loop of Figure 8, however, since the output frequency would have to vary more than 2:1.

Mixing is used because the digital phase detector has an upper frequency limit of about 10 MHz and many loops require direct locks at 20 MHz or more. Direct down-mixing does not change any loop characteristics except the sampling rate which restricts loop natural frequency to about $f_C/10$ in practical circuits. Although output frequency may be changed by varying either f_1 or f_C, the clock input is usually crystal controlled since it is of the same magnitude as f_D and more difficult to stabilize.

FIGURE 8

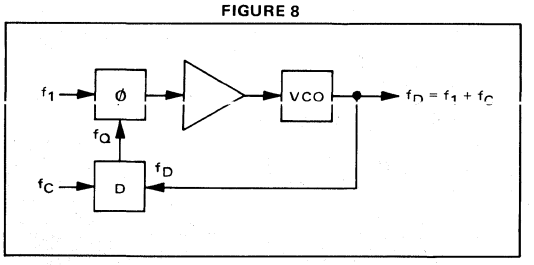
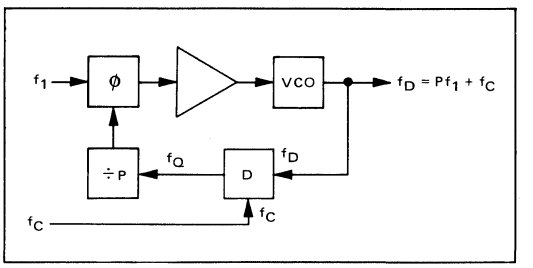


FIGURE 9



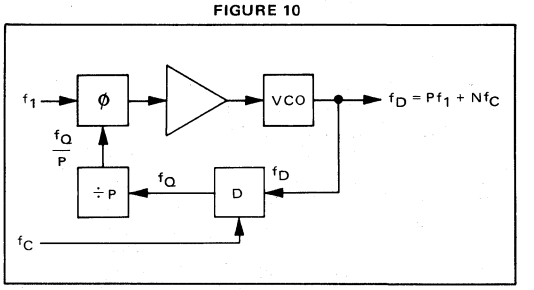
Combining a standard synthesis configuration with the mixer yields a circuit capable of high frequency operation at low cost (Figure 9), if the output frequency range is relatively small ($P_{max} - P_{min}$) $f_1 < f_C/2$. In fact the choice of harmonic or non-harmonic mixing is largely based on the availability of a suitable crystal or other reference source for f_C versus the needed frequency coverage. Considering all the restrictions on f_C, its value (and the maximum harmonic number N) are dictated by the following expressions:

$$N < \frac{f_{D(min)} - f_1}{2\,\Delta f_D} \qquad (1)$$

$$Nf_C = f_{D(min)} - f_1 \qquad (2)$$

where Δf_D = change in output frequency.

FIGURE 10



Using Equations (1) and (2) above the minimum value of f_C may be found for the circuit of Figure 10 and still get adequate frequency coverage. In this minimum configuration all necessary output frequencies may be generated by programming the "P" count string. But the divide number might bear no obvious relation to the output frequency such as often happens with non-mixing synthesizers.

DESIGN EXAMPLES

Example #1

Output Frequency: 48-54 MHz
Frequency Increments: 10 kHz
Using Equations (1) and (2), a minimum frequency (f_C) version can be designed:

$$f_1 = \text{increment} = 10\ \text{kHz}$$

$$N < \frac{48\ \text{MHz} - 10\ \text{kHz}}{2\ (54\text{-}48)\ \text{MHz}}$$

$$N < 4$$

Let N = 3

$$Nf_C = 47.99\ \text{MHz}$$

$$f_C = \frac{Nf_C}{N} = \frac{47.99}{3} = 15.99666\ \text{MHz}$$

$$f_C = 15.996666\ \text{MHz}$$

$$P_{min} = 1$$

$$P_{max} = \frac{\Delta f_D}{10\ \text{kHz}} + P_{min} \qquad (3)$$

$$P_{max} = \frac{6\ \text{MHz}}{10\ \text{kHz}} + P_{min}$$

$$P_{max} = 601$$

$$f_{Q(max)} = P_{max}\, f_1$$
$$= 6.01\ \text{MHz} \qquad (4)$$

Equation (4) above puts the divider string (divide-by-P) into a medium frequency situation where devices such as the MC4016/4316 may be utilized. Note that the divider number now indicates the channel selected rather than output frequency. That is, at f_D = 48.000 MHz, P = 1; at f_D = 54.000 MHz, P = 601.

If "proper" divide-by-P readings are desired for direct frequency readout a slight circuit modification is necessary. To enable a division at 48.000 MHz the first divide-by-P must be 100 rather than 1, and P_{max} would then be 700 to cover all 6 MHz. Recalculating $f_{Q(max)}$ from Equation 4 we still find that the 7 MHz maximum value allows use of the same components. The next question concerns the allowable range of f_Q in relation to f_C ($f_Q < f_C/2$). Since f_C is nearly 16 MHz, the range of f_Q can be contained. A cosmetic change to the most significant digit switch completes the design. Instead of reading 1 through 7 it must be modified to display 48 through 54.

Example #2

Output Frequency: 144-148 MHz
Frequency Increments: 10 kHz

$$f_1 = \text{increment} = 10\ \text{kHz}$$

$$N < \frac{144.00 - 0.01}{2\ (4)}$$

$$N < 18$$

Let N = 17

$$Nf_C = 144.00 - 0.01\ \text{MHz}$$
$$= 143.99$$

$$f_C = \frac{Nf_C}{N} = 8.470\ \text{MHz}$$

$$P_{min} = 1$$

$$P_{max} = \frac{4\ \text{MHz}}{10\ \text{kHz}} + 1$$
$$= 401$$

$$f_{Q(max)} = P_{max}\, f_1 = 4.01\ \text{MHz}$$

Maximum frequency seen by the divide-by-P chain is still well within the MC4016 rating.

When converting this synthesizer to one that needs frequency directly, a "1" is again added to the most significant digit (MSD). This results in a P_{min} of 100 to P_{max} of 500. In this example, however, $f_{Q(max)}$ is 5 MHz which easily exceeds $f_C/2$. To alleviate this difficulty, the "N" factor must be decreased in order to raise f_C to at least 10 MHz.

$$N < \frac{f_{D(min)} - f_1}{f_C}$$

Let f_C = 10 MHz

$$N < \sim 14.4$$

Let N = 14

$$Nf_C = 143.99\ \text{(from above)}$$

$$f_C = \frac{Nf_C}{N} = \frac{143.99}{14}$$

$$f_C = 10.28540\ \text{MHz} \qquad (5)$$

VCO RANGE RESTRICTIONS

As in all harmonically locked PLL's, it is possible for the loop to lock on the wrong harmonic if there is too wide a range in the VCO. This situation is shown in Figure 11 where the possible false lock areas are indicated near the (N - 1) and (N + 1) harmonic points. The problem of VCO restraint however is more than just making sure that output frequency f_D isn't able to go to B or A' (the closest false lock points). Actual operating limits are C and C', symmetrically placed frequencies corresponding to $f_{D(min)}$ about Nf_C and $f_{D(max)}$ about $(Nf+1/2)\ f_C$. If the VCO drops below C while the feedback counter is at P_{min} the phase detector will try to push f_D even lower, toward the stable condition at A (Figure 12). Likewise, at C' (when $P = P_{max}$) the tendency is for the loop to accelerate toward lockup at B' (Figure 13). When C or C' are exceeded the loop will "hang up" and not attain the proper lock.

FIGURE 11

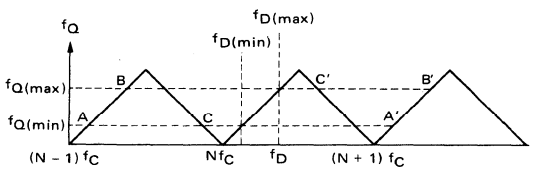


FIGURE 12

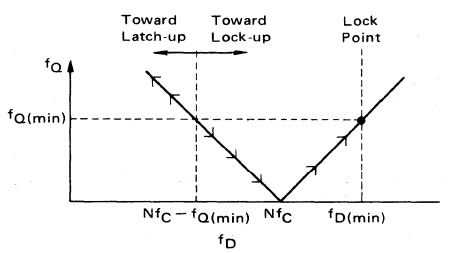
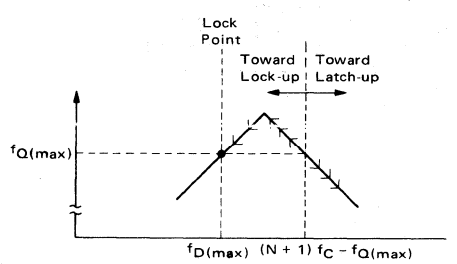
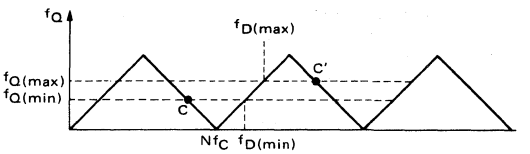


FIGURE 13



The VCO frequency constraints may be quite severe if the minimum f_C formulation is followed and the Nth harmonic is quite high. Where VCO constraint may pose a problem, decrease N below the maximum indicated by Equation (1) until sufficient room is generated by placing the operating range of f_Q on only a small part of the f_D slope (Figure 14). Note that f_C goes up as we approach the more idealized case (Equation 5).

FIGURE 14



The most likely reasons for a "latched up" state in a harmonic loop are turn-on transients and loop overshoot when changing frequency abruptly from one end of the range to the other.

SUMMARY OF SYNTHESIS PROCEDURE

1. Compute harmonic number N

$$N < \frac{f_{D(min)} - f_1}{2\,\Delta f_D}$$

where Δf_D = change in output frequency
f_1 = channel spacing

2. Compute minimum mixing frequency f_C

$$f_C = \frac{f_{D(min)} - f_1}{N}$$

3. Calculate feedback divider's maximum value

$$P_{max} = \frac{\Delta f_D}{f_1} + P_{min}$$

where $P_{min} = 1$ for minimum f_C.

4. Find maximum divide-by-P frequency

$$f_{Q(max)} = \Delta f_D + f_1$$

5. Calculate allowable VCO swing

$$Nf_C - f_1 < f_{VCO} < (N + 1)\ f_C - f_{Q(max)}$$

6. If the above constraints are too tight choose the next lower number for N and repeat steps 2 and 5 until satisfied.

4

SKIP-LOCK TUNING

Harmonic mixing provides an alternate means to frequency synthesis without the feedback divide-by-P network. In this instance the design objective is to provide a large frequency coverage with a set (and relatively wide) channel spacing. The configuration is identical to a single frequency PLL (Figure 15) except it operates in the harmonic mode and tuning is accomplished at the VCO. Output frequency is fixed as being f_1 above all harmonics of f_C. As the VCO is tuned through its range, the loop will acquire and lose signals spaced f_C apart. Since these must be some frequency for the phase detector to operate with, the output frequency cannot be a direct harmonic of f_C. This facet of the circuit often causes users to refer to f_1 as the "offset" frequency.

The value of f_1 is often dictated by output frequency and channel spacing requirements. However the relationship of f_1 to f_C has a large effect on the tunability both up and down the frequency range. If, for example, the loop were locked at point A (Figure 16) and B were the next desired point, then the VCO must be "dragged" from A to A′ before lock can be achieved. This frequency adjustment may be quite critical since the frequency difference between A′ and B is only $2f_1$. If the VCO is tuned past B the opportunity for lock has been passed.

On the other hand, in going from B to A, the upper end of the VCO control range must only cross A′ before the loop acquires frequency A. In either case it's apparent that the loop will not "jump" from one lock point to another and some indication of loop lock should be added. This is normally done by monitoring the VCO dc control line with a pair of comparators and noting when the line reaches its limits.

FIGURE 15

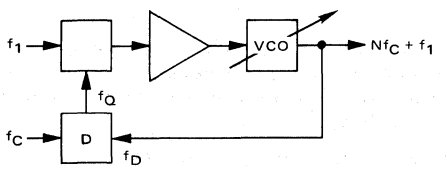
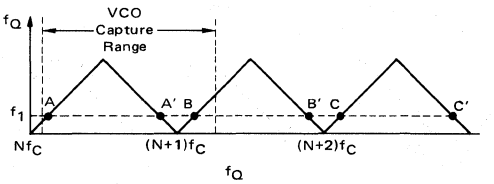


FIGURE 16

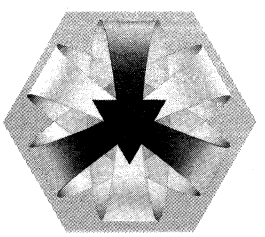


MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Ratings above which device life may be impaired:			
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8.0	Vdc
Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{IL} min	Vdc
Output Source Current	I_o	40	mAdc
Storage Temperature Range	T_{stg}	-55 to +125	°C
Recommended maximum ratings above which performance may be degraded:			
Operating Temperature Range	T_A	0 to +75	°C
DC Fan-Out* (Gates and Flip-Flops)	n	70	–

*AC fan-out is limited by desired system performance.

COUNTERS



COUNTER SELECTOR GUIDE

FUNCTION	SPEED (TYP) MHz	DEVICE #	TEMP RANGE	PACKAGE (CASE #)	LOGIC DIAGRAM FIGURE
TTL					
Programmable Modulus-N Decade Counter (÷0 thru 9)	*8.0	MC74416L,P (MC4016L,P)	0°C to +75°C	620,648	1
Programmable Modulus-N Hexadecimal Counter (÷0 thru 15)	*8.0	MC74418L,P (MC4018L,P)	0°C to +75°C	620,648	1
Programmable Modulus-N Decade Counter (÷0 thru 9)	*8.0	MC54416L (MC4316L)	−55°C to +125°C	620	1
Programmable Modulus-N Hexadecimal Counter (÷0 thru 15)	*8.0	MC54418L (MC4318L)	−55°C to +125°C	620	1
Universal Counter, (÷2 thru 12, except 7 & 11)	30	MC4023F,L,P	0°C to +75°C	607,632,646	2
Decade Counter (÷2, ÷5, ÷10)	20	MC5490F,L	−55°C to +125°C	607,632	3
Decade Counter (÷2, ÷5, ÷10)	20	MC7490F,L,P	0°C to +75°C	607,632,646	3
Counter Control Logic		**MC12014L**	**0°C to +75°C**	**620**	**4**
(*) Speed can be increased to 25 MHz (typ) when used in conjunction with MC12014					
MECL					
Bi-Quinary Counter (÷2, ÷5, ÷10)	325	MC1678L	0°C to +75°C	620	5
UHF Prescaler Type D Flip-Flop (÷2)	500	MC1690S	0°C to +75°C	617	6
Variable Modulus Prescaler (÷2 or ÷5, ÷6 or ÷10, ÷11 or ÷10, ÷12)	**225**	**MC12012L**	**0°C to +75°C**	**620**	**7**
Universal Hexadecimal counter (0 to 15)	*150	MC10136L	−30°C to +85°C	620	8
Universal BCD decade counter	*150	MC10137L	−30°C to +85°C	620	9
(*) When used as a prescaler, it is possible to extend the input frequency of the MC10136, 37 to over 200 MHz with the MC10231; to 300 MHz with the MC1670; or to over 500 MHz with the MC1690 and MC1670.					
CMOS					
Decade Counter-Divider (÷10) (÷N using MC14001)	5.0	MC14017AL	−55°C to +125°C	620	10
Decade Counter-Divider (÷10) (÷N using MC14001)	5.0	MC14017CL	−40°C to +85°C	620	10
Binary Counter ÷(2^{12})	10.0	MC14040AL	−55°C to +125°C	632	11
Binary Counter ÷(2^{12})	10.0	MC14040CL	−40°C to +85°C	632	11
BCD Presettable Up/Down Counter (÷10)	6.0	MC14510AL	−55°C to +125°C	620	12
BCD Presettable Up/Down Counter (÷10)	6.0	MC14510CL	−40°C to +85°C	620	12
Binary Up/Down Counter (÷16)	6.0	MC14516AL	−55°C to +125°C	620	13
Binary Up/Down Counter (÷16)	6.0	MC14516CL	−40°C to +85°C	620	13
Dual BCD Up Counter (÷10 or ÷100)	6.0	MC14518AL	−55°C to +125°C	620	14
Dual BCD Up Counter (÷10 or ÷100)	6.0	MC14518CL	−40°C to +85°C	620	14
Dual Binary Up Counter (÷16 or ÷256)	6.0	MC14520AL	−55°C to +125°C	620	14
Dual Binary Up Counter (÷16 or ÷256)	6.0	MC14520CL	−40°C to +85°C	620	14
BCD Programmable Divide by N (÷0 thru 9)	5.0	MC14522AL	−55°C to +125°C	620	15
BCD Programmable Divide by N (÷0 thru 9)	5.0	MC14522CL	−40°C to +85°C	620	15
Binary Programmable Divide by N (÷0 thru 15)	5.0	MC14526AL	−55°C to +125°C	620	15
Binary Programmable Divide by N (÷0 thru 15)	5.0	MC14526CL	−40°C to +85°C	620	15

5

Figure 1 – MC54416 • MC74416 Programmable Modulus N Decade Counter
MC54418 • MC74418 Programmable Modulus N Hexadecimal Counter

These devices are programmable, cascadable, modulo-N counters. The MC54416/74416 can be programmed to divide by any number (N) from 0 thru 9, the MC54418/74418 from 0 thru 15.

The parallel enable ($\overline{PE}$) input enables the parallel preset inputs D0 thru D3. All zeros are entered into the counter by applying a logic "0" level to the master reset (MR) and $\overline{PE}$ inputs. This causes the counter to stop counting (count = 0). All preset inputs are independent of the logic level of the Clock.

Modulo-N counters are useful in frequency synthesizers, in phase-locked loops, and in other applications where a simple method for frequency division is needed.

COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

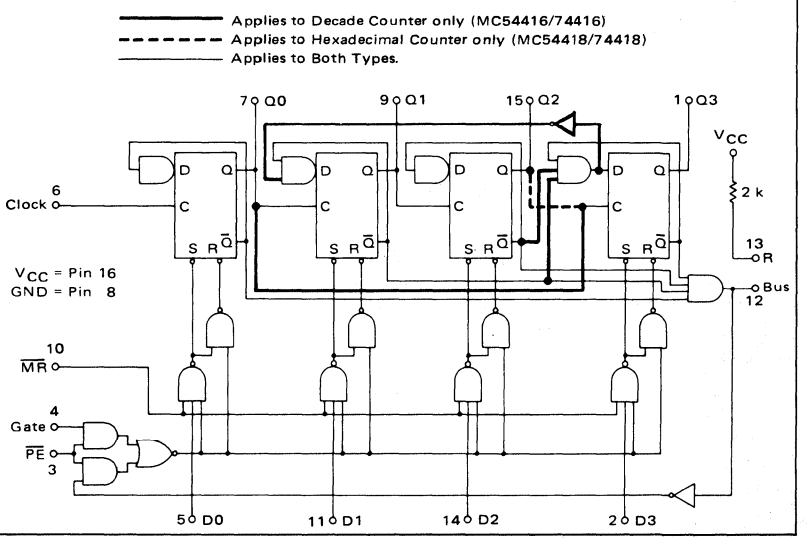
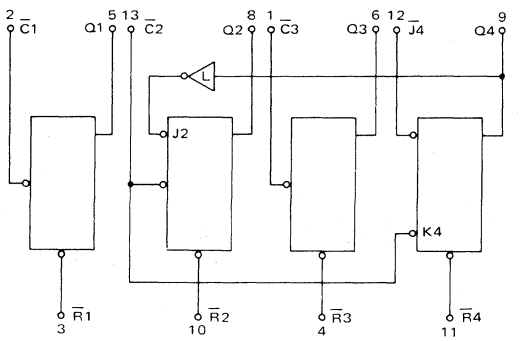


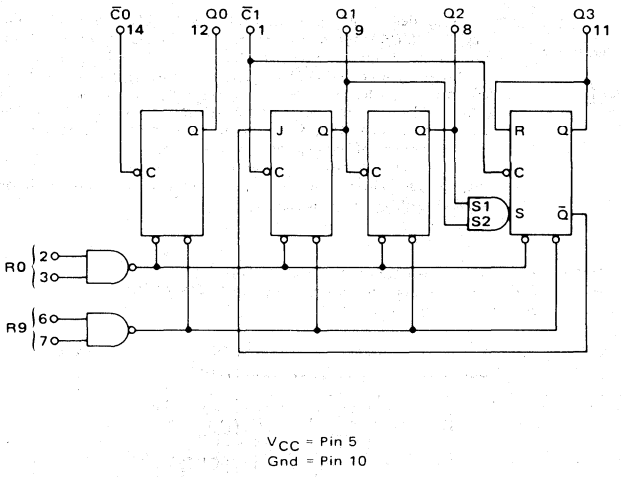
Figure 2 – MC4023 4-Bit Universal Counter



This device is a 4-bit counter with internally connected feedback. Inputs and outputs can be connected to count to any number between two and twelve except seven and eleven. Reset inputs are provided on each flip-flop to allow direct setting of the Q outputs to zero any time during the counting cycle.

Each flip-flop in the counter is built from high and low-level gates as shown by the logic diagram. The flip-flops and the feedback inverter are connected as shown by the block diagram to provide minimum power dissipation and maximum drive capability.

Figure 3 – MC5490 • MC7490 Decade Counter



V_{CC} = Pin 5
Gnd = Pin 10

RESET/COUNT TRUTH TABLE

R0		R9		OUTPUT			
Pin 2	Pin 3	Pin 6	Pin 7	Q3	Q2	Q1	Q0
1	1	0	X	0	0	0	0
1	1	X	0	0	0	0	0
X	X	1	1	1	0	0	1
X	0	X	0	COUNT			
0	X	0	X	COUNT			
0	X	X	0	COUNT			
X	0	0	X	COUNT			

X = Don't care.

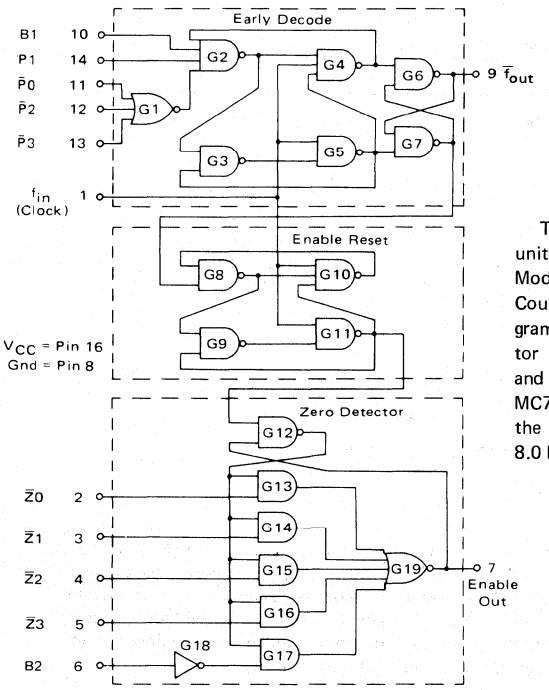
COUNT SEQUENCE TRUTH TABLE

COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Q0 connected to C̄1

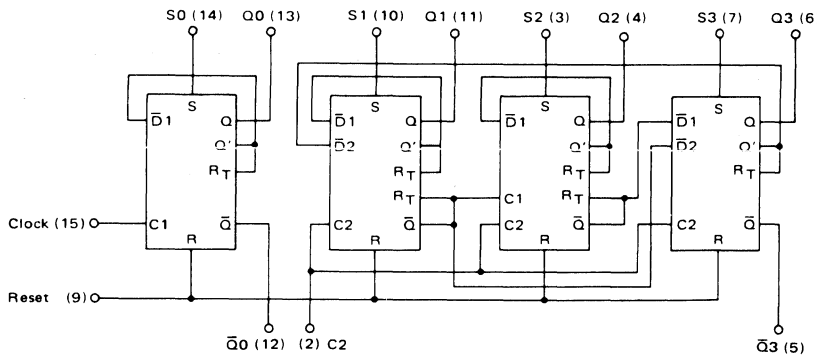
This 4-bit counter is comprised of a divide-by-two section and a divide-by-five section. These sections can be used independently, or can be connected to perform the counting function or the simple divide-by-ten function with an output duty cycle of 50%. Two sets of direct RESET inputs are provided to allow setting all outputs to a logic "0" or to the BCD count of 9.

Figure 4 – MC12014 Counter Control Logic



The MC12014 monolithic counter control logic unit is designed for use with the MC12012 Two-Modulus Prescaler and the MC74416 Programmable Counter to accomplish direct high-frequency programming. The MC12014 consists of a zero detector which controls the modulus of the MC12012, and an early decode function which controls the MC74416. The early decode feature also increases the useful frequency range of the MC74416 from 8.0 MHz to 25 MHz.

Figure 5 — MC1678 • MC1679 Bi-Quinary Counter



Number in parenthesis denotes pin number for L package (Case 620).

BCD

(Clock connected to C1 and Q̄0 connected to C2)

COUNT	Q0	Q1	Q2	Q3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

BI-QUINARY

(Clock connected to C2 and Q̄3 connected to C1)

COUNT	Q1	Q2	Q3	Q0
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	L	L	L	H
6	H	L	L	H
7	L	H	L	H
8	H	H	L	H
9	L	L	H	H

R-S

C	R	S	Q_{n+1}
ϕ	L	L	Q_n
ϕ	H	L	H
ϕ	L	H	H
ϕ	H	H	ND

ϕ = Don't Care
ND = Not Defined

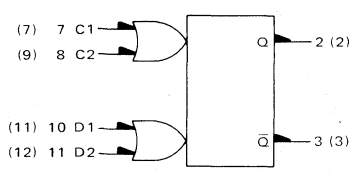
The MC1678/1679 is a four-bit counter capable of divide-by-two, divide-by-five, or divide-by-10 functions. When used independently, the divide-by-two section will toggle at 350 MHz typically, while the divide-by-five section will toggle at 325 MHz typically. Clock inputs trigger on the positive going edge of the clock pulse.

Set and Reset inputs override the clock, allowing asynchronous "set" or "clear". Individual Set and common Reset inputs are provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all bits.

5

Figure 6 — MC1690 UHF Prescaler "D" Flip Flop

POSITIVE LOGIC



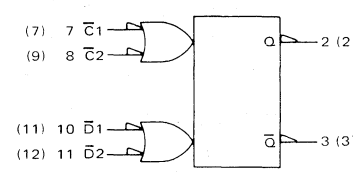
TRUTH TABLE

C	D	Q_{n+1}
L	ϕ	Q_n
H	ϕ	Q_n
⎍	L	L
⎍	H	H

C = C1 + C2
D = D1 + D2

ϕ = Don't Care

NEGATIVE LOGIC



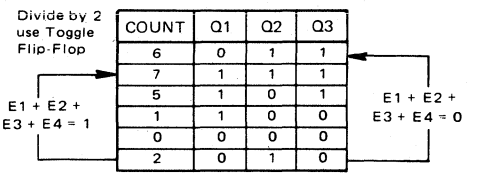
The MC1690 is a high speed D master-slave flip-flop capable of toggle rates over 500 MHz. Designed primarily for high speed prescaling applications in communications and instrumentation, this device employs two data inputs, two clock inputs and complementary Q and Q̄ outputs.

It is a higher frequency replacement for the MC1670 (350 MHz) D flip-flop. No set or reset inputs are provided and an extra data input is provided on pin 11.

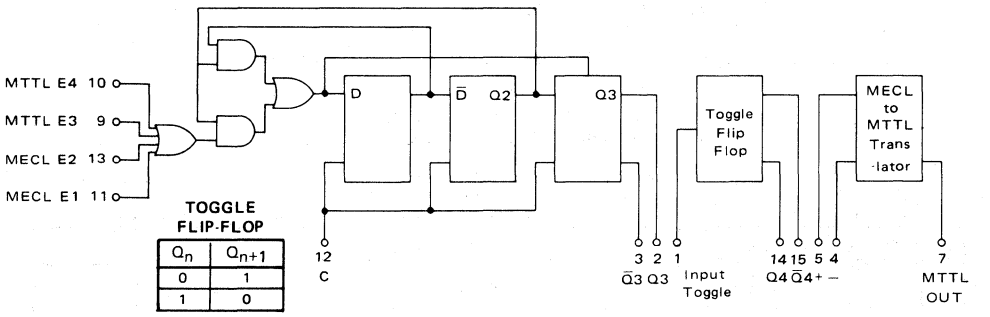
When used with the MC1678, the MC1690 provides a decade counter capable of 500 MHz operation.

Figure 7 — MC12012 Variable Modulus Prescaler

The MC12012 is a two-modulus prescaler which consists of three functional blocks: 1) a controllable divide by 5/divide by 6 prescaler; 2) a divide by 2 prescaler; and 3) a MECL to MTTL translator. When used with the MC12014 Counter Control Logic function and the MC4016 programmable counter, a divide by N programmable counter can be constructed for operation to 200 MHz. This arrangement is especially useful in frequency synthesizer applications.



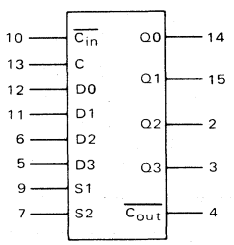
COUNT	Q1	Q2	Q3
6	0	1	1
7	1	1	1
5	1	0	1
1	1	0	0
0	0	0	0
2	0	1	0



TOGGLE FLIP-FLOP

Q_n	Q_{n+1}
0	1
1	0

Figure 8 — MC10136 Universal Hexadecimal Counter



FUNCTION SELECT TABLE

S1	S2	Operating Mode
L	L	Preset (Program)
L	H	Increment (Count Up)
H	L	Decrement (Count Down)
H	H	Hold (Stop Count)

SEQUENTIAL TRUTH TABLE*

INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	$\overline{\text{Carry In}}$	Clock **	Q0	Q1	Q2	Q3	$\overline{\text{Carry Out}}$
L	L	L	L	H	H	L	H	L	L	H	H	L
L	H	ϕ	ϕ	ϕ	ϕ	L	H	H	L	H	H	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	L	H	H	H	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	H	H	H	H	L
L	H	ϕ	ϕ	ϕ	ϕ	H	H	H	H	H	H	H
H	H	ϕ	ϕ	ϕ	ϕ	L	H	H	H	H	H	L
H	H	ϕ	ϕ	ϕ	ϕ	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	H	H	L	L	L
H	L	ϕ	ϕ	ϕ	ϕ	L	H	L	H	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	H	L	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	L	L	L	L	L
H	L	ϕ	ϕ	ϕ	ϕ	L	H	H	H	H	H	H

ϕ = Don't care.

* Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.

** A clock H is defined as a clock input transition from a low to a high logic level.

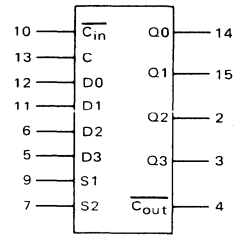
The MC10136 is a high speed synchronous counter that can count up, count down, preset, or stop count at frequencies exceeding 100 MHz. This binary counter is useful in high speed central processors and peripheral controllers, minicomputers, high speed digital communications equipment and instrumentation. The flexibility of this device allows the designer to use one basic counter for most applications, and the synchronous count feature makes the MC10136 suitable for either computers or instrumentation.

Three control lines (S1, S2, and Carry In) determine the operation mode of the counter. Lines S1 and S2 determine one of four operations; preset (program), increment (count up), decrement (count down), or hold (stop count). Note that in the preset mode a clock pulse is necessary to load the counter, and the information present on the data inputs (D0, D1, D2, and D3) will be entered into the counter. Carry Out goes low on the terminal count, or when the counter is being preset.

When an output is not needed, it can be left open to conserve system power. (The open emitter output will require no power if left open). The counter changes state only on the positive going edge of the clock. Any other input may change at any time except during the positive transition of the clock.

A prescaler can be constructed using the MC10136 in conjunction with the MC10231 which will operate at over 200 MHz input frequency. A 500 MHz prescaler is possible using an MC1690 500 MHz D Flip-Flop, an MC1670 300 MHz D Flip-Flop, and the MC10136.

Figure 9 – MC10137 Universal BCD Decade Counter



FUNCTION SELECT TABLE

S1	S2	Operating Mode
L	L	Preset (Program)
L	H	Increment (Count Up)
H	L	Decrement (Count Down)
H	H	Hold (Stop Count)

SEQUENTIAL TRUTH TABLE*

INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	$\overline{\text{Carry In}}$	Clock **	Q0	Q1	Q2	Q3	$\overline{\text{Carry Out}}$
L	L	H	H	H	L	ϕ	H	H	H	H	L	H
L	H	ϕ	ϕ	ϕ	ϕ	I	H	L	I	I	H	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	H	L	L	H	L
L	H	ϕ	ϕ	ϕ	ϕ	L	H	L	L	L	L	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	H	L	L	L	H
L	H	ϕ	ϕ	ϕ	ϕ	H	H	H	L	L	L	H
H	H	ϕ	ϕ	ϕ	ϕ	L	H	H	L	L	L	H
L	L	H	H	L	L	ϕ	H	H	H	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	L	H	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	H	L	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	L	L	L	L	L

ϕ = Don't care.

* Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.

** A clock H is defined as a clock input transition from a low to a high logic level.

The MC10137 is a high speed synchronous counter that can count up, count down, preset, or stop count at frequencies exceeding 100 MHz. This decade counter is useful in high speed central processors and peripheral controllers, minicomputers, high speed digital communications equipment and instrumentation. The flexibility of this device allows the designer to use one basic counter for most applications. The synchronous count feature makes the MC10137 suitable for either computers or instrumentation.

Three control lines (S1, S2, and $\overline{\text{Carry In}}$) determine the operation mode of the counter. Lines S1 and S2 determine one of four operations; preset (program), increment (count up), decrement (count down), or hold (stop count). Note that in the preset mode a clock pulse is necessary to load the counter, and the information present on the data inputs (D0, D1, D2, and D3) will be entered into the counter. $\overline{\text{Carry Out}}$ goes low on the terminal count or when the counter is being preset.

When an output is not needed, it can be left open to conserve system power. (The open emitter output will require no power if left open.) The counter changes state only on the positive going edge of the clock. Any other input may change at any time except during the positive transition of the clock. The sequence for counting out of improper states is as shown in the State Diagrams.

A prescaler can be constructed using the MC10137 in conjunction with the MC10231 which will operate at over 200 MHz input freuqency. A 500 MHz prescaler is possible using an MC1690 500 MHz D Flip-Flop, an MC1670 300 MHz D Flip-Flop, and the MC10137.

5

Figure 10 – MC14017 Decade Counter-Divider

The MC14017AL/CL is a five-stage Johnson decade counter with built-in code converter. High-speed operation and spike-free outputs are obtained by use of a Johnson decade counter design. The ten decoded outputs are normally low, and go high only at their appropriate decimal time period. The output changes occur on the positive-going edge of the clock pulse. This part can be used in frequency division applications as well as decade counter or decimal decode display applications.

- Fully Static Operation
- DC Clock Input Circuit Allows Slow Rise Times
- Carry Out Output for Cascading
- 10 MHz (typical) Operation @ V_{DD} = 10 Vdc
- Divide-by-N Counting when used with MC14001 NOR Gate
- Pin-for-Pin Equivalent to CD4017A

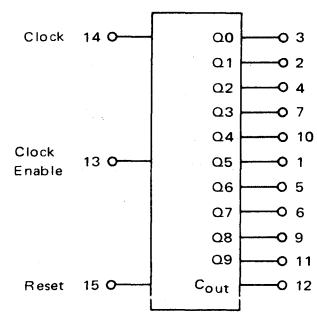
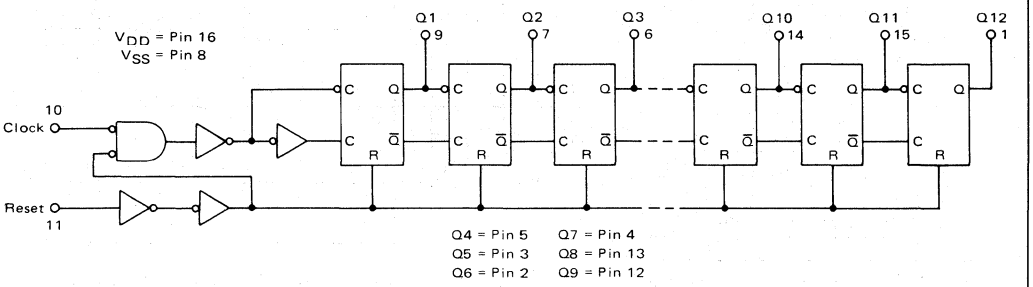


Figure 11 — MC14040 12-Bit Binary Counter



TRUTH TABLE

$\overline{\text{CLOCK}}$	RESET	OUTPUT STATE
⌐	0	No Change
¬	0	Advance to next state
X	1	All Outputs are low

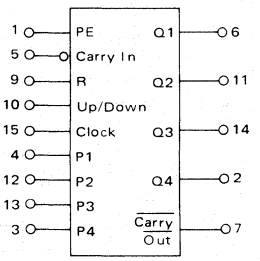
X = Don't Care

The MC14040AL/CL 12-stage binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 12 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency-dividing circuits.

5

Figure 12 — MC14510 BCD Presettable Up/Down Counter

BLOCK DIAGRAM



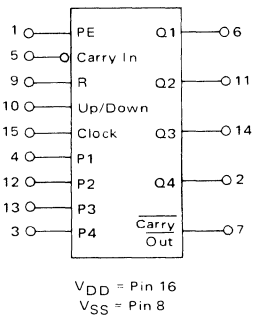
TRUTH TABLE

$\overline{\text{CARRY IN}}$	UP/DOWN	PRESET ENABLE	RESET	ACTION
1	X	0	0	No Count
0	1	0	0	Count Up
0	0	0	0	Count Down
X	X	1	0	Preset
X	X	X	1	Reset

X = Don't Care

The MC14510AL/CL BCD up/down counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The counter consists of type D flip-flop stages with a gating structure to provide type T flip-flop capability. The counter can be cleared by applying a high level on the Reset line. This complementary MOS counter finds primary use in up/down and difference counting and frequency synthesizer applications where low power dissipation and/or high noise immunity is desired. It is also useful in A/D and D/A conversion and for magnitude and sign generation.

Figure 13 – MC14516 Binary Up/Down Counter



The MC14516AL/CL is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This complementary MOS circuit finds primary use where low power dissipation and/or high noise immunity is desired.

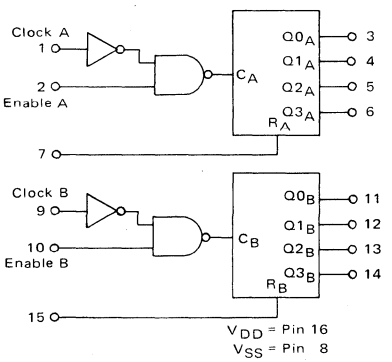
This binary presettable up/down counter may be used as a counting/frequency synthesizer, in A/D and D/A conversion, for up/down counting, for magnitude and sign generation, and for difference counting.

TRUTH TABLE

$\overline{\text{CARRY IN}}$	UP/DOWN	PRESET ENABLE	RESET	ACTION
1	X	0	0	No Count
0	1	0	0	Count Up
0	0	0	0	Count Down
X	X	1	0	Preset
X	X	X	1	Reset

X = Don't Care

Figure 14 – MC14518 • MC14520 Dual BCD or Dual Binary Up Counters



TRUTH TABLE

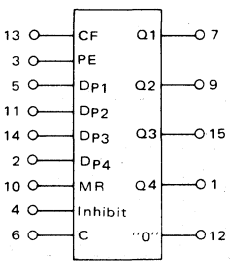
CLOCK	ENABLE	RESET	ACTION
↑	1	0	Increment Counter
0	↓	0	Increment Counter
↓	X	0	No Change
X	↑	0	No Change
↑	0	0	No Change
1	↓	0	No Change
X	X	1	Q0 thru Q3 = 0

X = Don't Care

The MC14518AL/CL dual BCD counter and the MC14520AL/CL dual binary counter are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each consists of two identical, independent, internally synchronous 4-stage counters. The counter stages are type D flip-flops, with interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition as required when cascading multiple stages. Each counter can be cleared by applying a high level on the Reset line. In addition, the MC14518 will count out of all undefined states within two clock periods. These complementary MOS up counters find primary use in multi-stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity.

Figure 15 – MC14522 • MC14526 BCD Programmable Divide by N 4-Bit Counter

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLES

MC14522

COUNT	OUTPUT Q4	Q3	Q2	Q1
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

MC14526

COUNT	OUTPUT Q4	Q3	Q2	Q1
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

The MC14522AL/CL BCD counter and the MC14526AL/CL binary counter are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure.

These devices are programmable, cascadable down counters with a decoded "0" state output for divide-by-N applications. In single stage applications the "0" output is applied to the Preset Enable input. The Cascade Feedback input allows cascade divide-by-N operation with no additional gates required. The Master Reset function provides synchronous initiation of divide-by-N cycles. The Clock Inhibit input allows disabling of the pulse counting function.

These complementary MOS counters can be used in frequency synthesizers, phase-locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

5

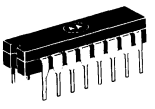
PROGRAMMABLE MODULO-N COUNTERS

MC54416 • MC74416
(MC4316) (MC4016)

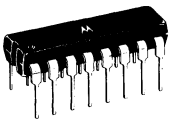
MC54417 • MC74417

MC54418 • MC74418
(MC4318) (MC4018)

MC54419 • MC74419



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC74416 thru MC74419 only

The monolithic devices are programmable, cascadable, modulo-N-counters. The MC54416/74416 can be programmed to divide by any number (N) from 0 thru 9, the MC54418/74418 from 0 thru 15. The MC54417/74417 consists of a modulo 2 counter which can be programmed to divide by 0 or 1 and a modulo 5 counter which can be programmed to divide by any number from 0 to 4. The MC54419/74419 contains two modulo 4 counters which can be programmed to divide by any number from 0 to 3.

The parallel enable ($\overline{PE}$) input enables the parallel data inputs D0 thru D3. All zeros are entered into the counter by applying a logic "0" level to the master reset ($\overline{MR}$) and $\overline{PE}$ inputs. This causes the counter to stop counting (count = 0). All data inputs are independent of the logic level of the Clock.

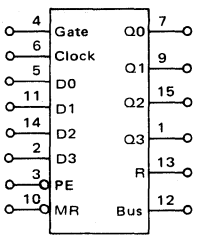
Modulo-N counters are useful in frequency synthesizers, in phase-locked loops, and in other applications where a simple method for frequency division is needed.

All Types:

Input Loading Factor:
Clock, $\overline{PE}$ = 2
D0, D1, D2, D3, Gate = 1
$\overline{MR}$ = 4
Output Loading Factor = 8

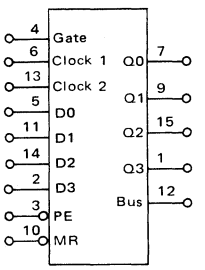
Total Power Dissipation = 250 mW typ/pkg
Propagation Delay Time:
Clock to Q3 = 50 ns typ
Clock to Bus = 35 ns typ

MC54416/74416
MC54418/74418



V_{CC} = Pin 16
Gnd = Pin 8

MC54417/74417
MC54419/74419



V_{CC} = Pin 16
Gnd = Pin 8

MC54416/74416

COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

MC54418/74418

COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

MC54417/74417

COUNT	OUTPUT
	Q0
1	1
0	0

COUNT	OUTPUT		
	Q3	Q2	Q1
4	1	0	0
3	0	1	1
2	0	1	0
1	0	0	1
0	0	0	0

MC54419/74419

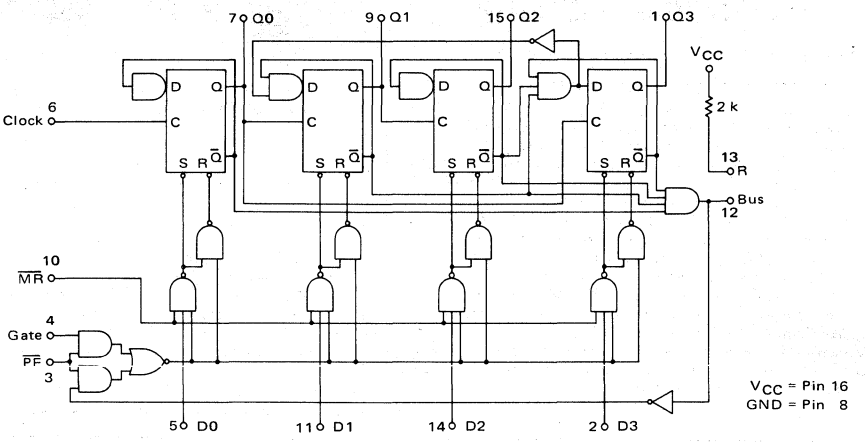
COUNT	OUTPUT	
	Q1	Q0
3	1	1
2	1	0
1	0	1
0	0	0

COUNT	OUTPUT	
	Q3	Q2
3	1	1
2	1	0
1	0	1
0	0	0

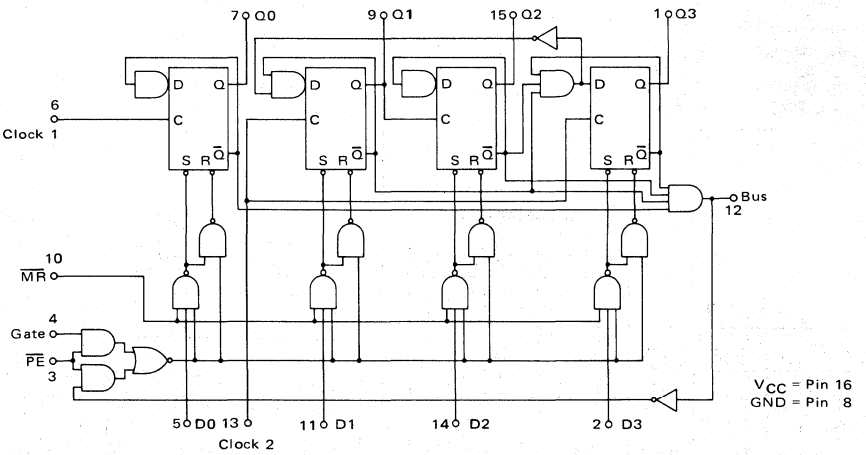
MC544XX/744XX is exact replacement for MC43XX/40XX number shown.

LOGIC DIAGRAMS

MC54416/74416

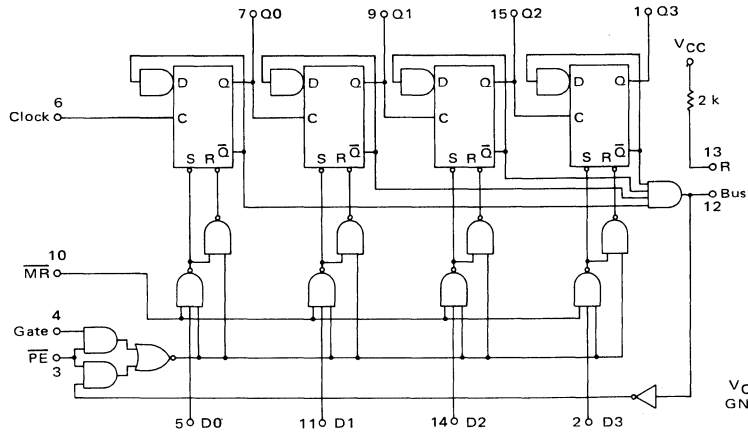


MC54417/74417

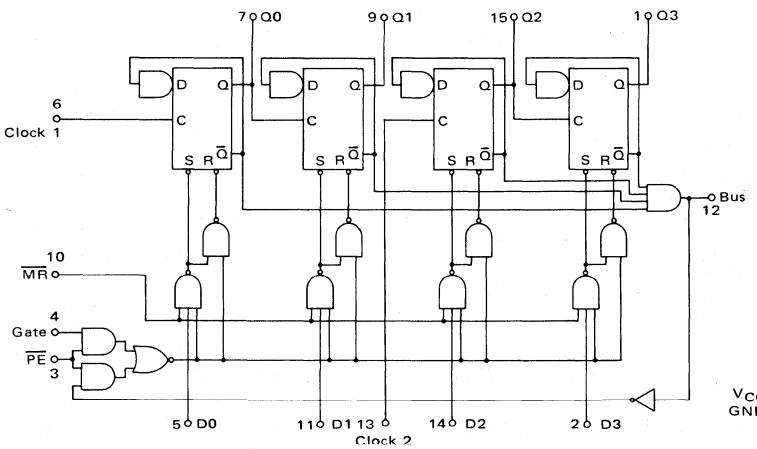


LOGIC DIAGRAMS (continued)

MC54418/74418



MC54419/74419



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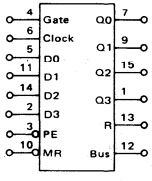
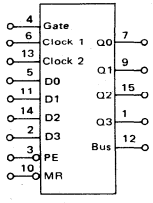
ELECTRICAL CHARACTERISTICS

Tests are shown for one output only. Others are tested in the same manner.

MC54416/74416
MC54418/74418



MC54417/74417
MC54419/74419



	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES													
		mA					Volts								
		I_{OL1}	I_{OL2}	I_{OL3}	I_{OH}	I_{IC}	V_{IL}	V_{IH}	V_{IHH}	V_{ILT}	V_{IHT}	V_{CC}	V_{CCL}	V_{CCH}	
MC54416-54419	-55°C	12.8	13.8	9.6	-1.6	–	0.4	2.4	5.5	0.8	2.0	5.0	4.5	5.5	
	+25°C	12.8	13.8	9.6	-1.6	-10	0.4	2.4	5.5	0.8	2.0	5.0	4.5	5.5	
	+125°C	12.8	13.8	9.6	-1.6	–	0.4	2.4	5.5	0.8	2.0	5.0	4.5	5.5	
MC74416-74419	0°C	12.8	13.8	9.6	-1.6	–	0.4	2.5	5.5	0.8	2.0	5.0	4.75	5.25	
	+25°C	12.8	13.8	9.6	-1.6	-10	0.4	2.5	5.5	0.8	2.0	5.0	4.75	5.25	
	+75°C	12.8	13.8	9.6	-1.6	–	0.4	2.5	5.5	0.8	2.0	5.0	4.75	5.25	

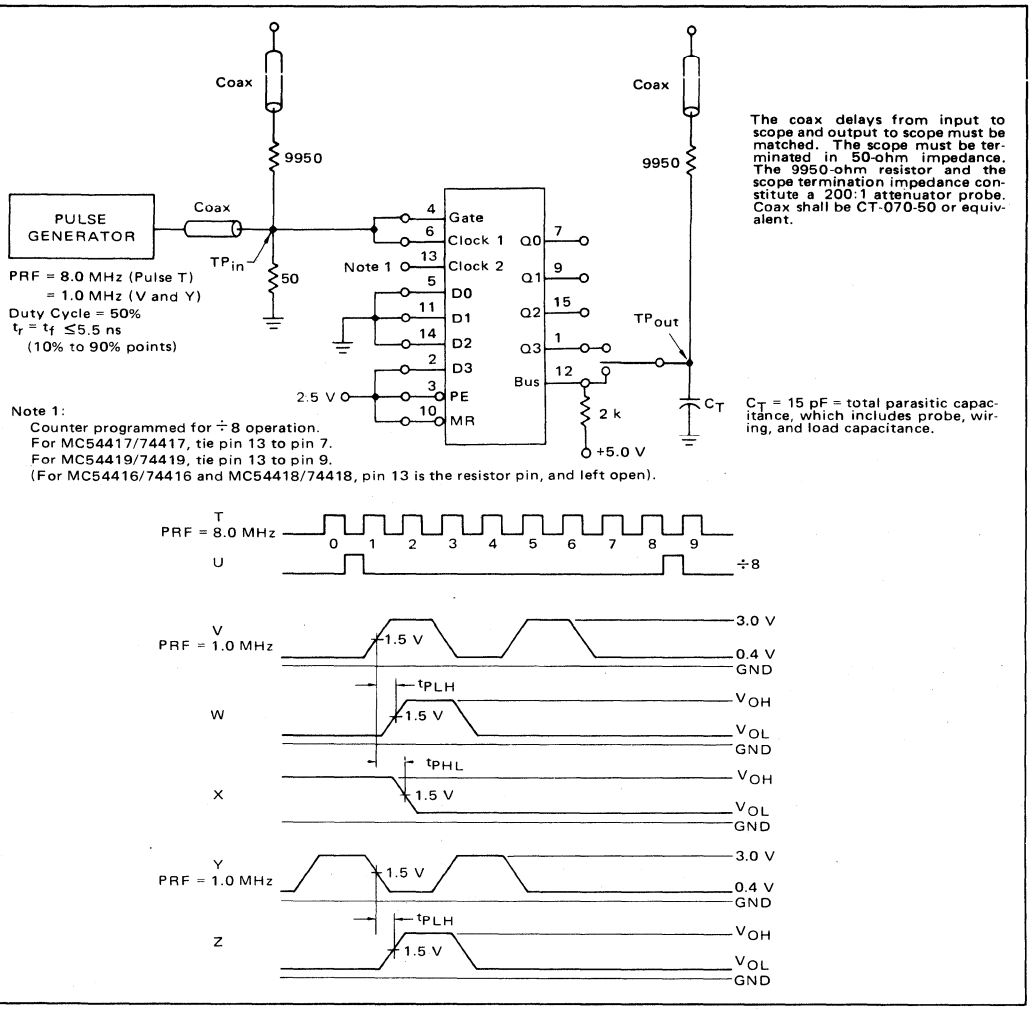
Characteristic	Symbol	Pin Under Test	MC54416-54419 Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC74416-74419 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OL3}	I_{OH}	I_{IC}	V_{IL}	V_{IH}	V_{IHH}	V_{ILT}	V_{IHT}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																													
Forward Current	I_{IL1}	2	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	mAdc	–	–	–	–	–	2	10	–	–	–	–	–	16	3,8
		3	–	-3.2	–	-3.2	–	-3.2	–	-3.2	–	-3.2	–	-3.2		–	–	–	–	–	3	4	–	–	–	–	–		8,12
		4	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6		–	–	–	–	–	4	3	–	–	–	–	–		8
		5	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6		–	–	–	–	–	5	10	–	–	–	–	–		3,8
		6	–	-3.2	–	-3.2	–	-3.2	–	-3.2	–	-3.2	–	-3.2		–	–	–	–	–	6	–	–	–	–	–	–		8
		10	–	-6.4	–	-6.4	–	-6.4	–	-6.4	–	-6.4	–	-6.4		–	–	–	–	–	10	2,5,11,14	–	–	–	–	–		3,8
		11	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6		–	–	–	–	–	11	10	–	–	–	–	–		
		14	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6		–	–	–	–	–	14	10	–	–	–	–	–		
	I_{IL2}	2	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	mAdc	–	–	–	–	–	2	10	–	–	–	–	16	–	3,8
		3	–	-2.8	–	-2.8	–	-2.8	–	-2.8	–	-2.8	–	-2.8		–	–	–	–	–	3	4	–	–	–	–		–	8,12
		4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4		–	–	–	–	–	4	3	–	–	–	–		–	8
		5	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4		–	–	–	–	–	5	10	–	–	–	–		–	3,8
		6*	–	-2.8	–	-2.8	–	-2.8	–	-2.8	–	-2.8	–	-2.8		–	–	–	–	–	6	–	–	–	–	–		–	8
		10	–	-5.6	–	-5.6	–	-5.6	–	-5.6	–	-5.6	–	-5.6		–	–	–	–	–	10	2,5,11,14	–	–	–	–		–	3,8
		11	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4		–	–	–	–	–	11	10	–	–	–	–		–	
		14	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4	–	-1.4		–	–	–	–	–	14	10	–	–	–	–		–	
Leakage Current	I_{IH}	2	–	40	–	40	–	40	–	40	–	40	–	40	μAdc	–	–	–	–	–	–	2	–	–	–	–	–	16	8,10
		3	–	80	–	80	–	80	–	80	–	80	–	80		–	–	–	–	–	–	3	–	–	–	–	–		4,8
		4	–	40	–	40	–	40	–	40	–	40	–	40		–	–	–	–	–	–	4	–	–	–	–	–		3,8
		5	–	40	–	40	–	40	–	40	–	40	–	40		–	–	–	–	–	–	5	–	–	–	–	–		8,10
		6	–	80	–	80	–	80	–	80	–	80	–	80		–	–	–	–	–	–	6	–	–	–	–	–		8
		10	–	160	–	160	–	160	–	160	–	160	–	160		–	–	–	–	–	–	10	–	–	–	–	–		2,5,8,11,14
		11	–	40	–	40	–	40	–	40	–	40	–	40		–	–	–	–	–	–	11	–	–	–	–	–		8,10
		14	–	40	–	40	–	40	–	40	–	40	–	40		–	–	–	–	–	–	14	–	–	–	–	–		8,10
	I_{IHH}	2	1.0	–	1.0	–	1.0	–	1.0	–	1.0	–	1.0	–	mAdc	–	–	–	–	–	–	–	2	–	–	–	–	16	8,10
		3		–		–		–		–		–		–		–	–	–	–	–	–	–	3	–	–	–	–		4,8
		4		–		–		–		–		–		–		–	–	–	–	–	–	–	4	–	–	–	–		3,8
		5		–		–		–		–		–		–		–	–	–	–	–	–	–	5	–	–	–	–		8,10
		6		–		–		–		–		–		–		–	–	–	–	–	–	–	6	–	–	–	–		8
		10		–		–		–		–		–		–		–	–	–	–	–	–	–	10	–	–	–	–		2,5,8,11,14
		11		–		–		–		–		–		–		–	–	–	–	–	–	–	11	–	–	–	–		8,10
		14		–		–		–		–		–		–		–	–	–	–	–	–	–	14	–	–	–	–		8,10
Clamp Voltage	V_{IC}	2**	–	–	–	-1.5	–	–	–	–	–	-1.5	–	–	Vdc	–	–	–	–	2	–	–	–	–	–	–	16	–	8
Output																													
Output Voltage	V_{OL}	1	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	1	–	–	–	–	–	–	–	2,3,5,11,14	–	–	16	–	8
		1	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4		–	1	–	–	–	–	–	–	2,3,5,11,14	–	–	–	16	
		12	–	0.5	–	0.5	–	0.5	–	0.5	–	0.5	–	0.5		–	–	12	–	–	–	–	–	3	2,5,11,14	–	16	–	
	V_{OH}	1	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	–	–	1	–	–	–	–	3	2,5,11,14	–	16	–	8
Short-Circuit Current	I_{OS}	1	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	mAdc	–	–	–	–	–	3	2,5,11,14	–	–	–	16	–	–	1,8
		13#	-1.8	-3.8	-1.8	-3.8	-1.8	-3.8	-1.8	-3.8	-1.8	-3.8	-1.8	-3.8	mAdc	–	–	–	–	–	–	–	–	–	–	16	–	–	8,13
Power Requirements (Total Device)																													
Power Supply Drain	I_{CC}	16	–	–	–	65	–	–	–	–	–	65	–	–	mAdc	–	–	–	–	–	–	–	–	–	–	16	–	–	8

*For MC54417/74417 and MC54419/74419, also test pin 13 using the same procedure except V_{IL} applied to pin 13.

**Test all inputs in the same manner.

#Test applies only to MC54416/74416 and MC54418/74418.

SWITCHING TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS



SWITCHING TIME TEST PROCEDURES (T_A = 25°C)
(Letters shown in test columns refer to waveforms.)

TEST	SYMBOL	INPUT				OUTPUT		LIMITS		
		Clock Pin 6	Gate Pin 4	D0, D1, D2 Pins 5,11,14	D3, $\overline{PE}$, $\overline{MR}$ Pins 2,3,10	Bus Pin 12	Q3 Pin 1	Min	Max	Unit
Toggle Frequency (Check before measuring propagation delay.)	f_{tog}	T	T	Gnd	2.5 V	–	U	8.0	–	MHz
Propagation Delay Clock to Bus	t_{PLH}	V	V	Gnd	2.5 V	W	–	–	65	ns
Propagation Delay Gate to Q3	t_{PLH}	Y	Y	Gnd	2.5 V	–	Z	–	35	ns
Propagation Delay Clock 1 to Q3 MC54416,17/74416,17 MC54418,19/74418,19	t_{PHL}	V	V	Gnd	2.5 V	–	X	– –	45 78	ns ns

OPERATING CHARACTERISTICS

MC54416/74416, MC54418/74418

Operation of both counters is essentially the same. The MC54416/74416 has a maximum modulus of ten while the MC54418/74418 is capable of dividing by up to sixteen. Minor differences in the programming procedure will be covered in the discussion of cascaded stages.

Suitable connections for operating a single stage are shown in Figure 1, as well as appropriate waveforms. The desired modulus is applied to the data inputs D0, D1, D2, and D3 in binary (MC74418) or binary coded decimal (MC74416) positive logic format. If a number greater than nine (BCD 1001) is applied to the MC74416, it treats the most significant bit position as a zero; if for example, binary fourteen (1110) were applied to an MC74416, the counter would divide by six. BCD eight is programmed in Figure 1. As $\overline{PE}$ is taken low the states on the parallel inputs are transferred to their respective outputs. Subsequent positive transitions of the input clock will decrement the counter until the all zero state is detected by the bus gate. The resulting positive transition of the bus line is internally inverted and fed back to the preset gating circuitry but does not yet preset the counter since the gate-clock input is still high. As the clock returns to the low state the counter is set to the programmed state, taking the bus line low. The net result is one positive pulse on the bus line for every N clock pulses. The output pulse width is approximately equal to one clock pulse high time.

Operation will continue in this fashion until the data on the programmable inputs is changed. Since the preset circuitry is inhibited except when the counter is in the zero state, preset data may be changed while clocking is occurring. If it is necessary to enter a new number before the counter has reached zero this can be done by momentarily taking $\overline{PE}$ low. Countdown will continue from the new number on the next positive clock transition.

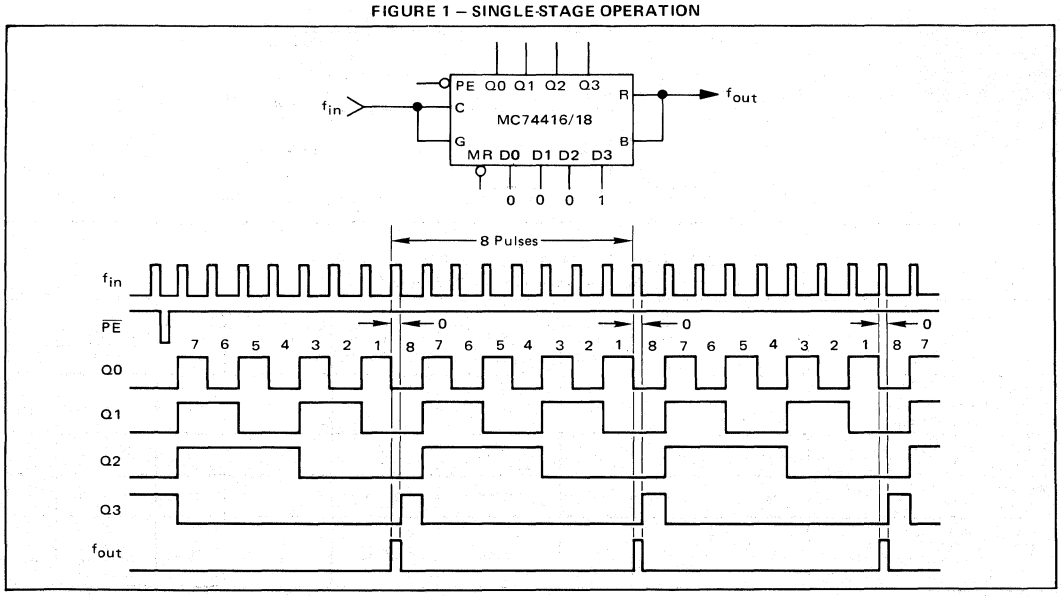
The counters can be made to divide by 10 (MC74416) or 16 (MC74418) by inhibiting the preset logic. This may be done by either holding the gate input high or by holding the bus line low.

The normal connections for cascading stages are indicated in Figure 2, with the appropriate waveforms. Note that the gate input of each stage is connected to the clock; all bus outputs are tied to one of the internal pullup resistors, R. The total modulus for cascaded MC74416's is determined from $N_T = N_0 + 10N_1 + 100N_2 + \ldots$; N_T for MC74418's is given by $N_T = N_0 + 16N_1 + 256N_2 + \ldots$ Stated another way, the BCD equivalent of each decimal digit is applied to respective MC74416 stages while the data inputs of the MC74418 stages are treated as part of one long binary number. The difference in programming is illustrated in Figure 2 where $N_T = 245$ is coded for both counter types.

Cascaded operation can be further clarified by referring to the timing diagram of Figure 2. For the MC74416, counting begins with the first positive clock transition after the data has been set in. After the five clock pulses, the least-significant stage has been counted down to zero. The bus line does not go high at this time since the three bus terminals are wire-ORed and the other two stages are not in

5

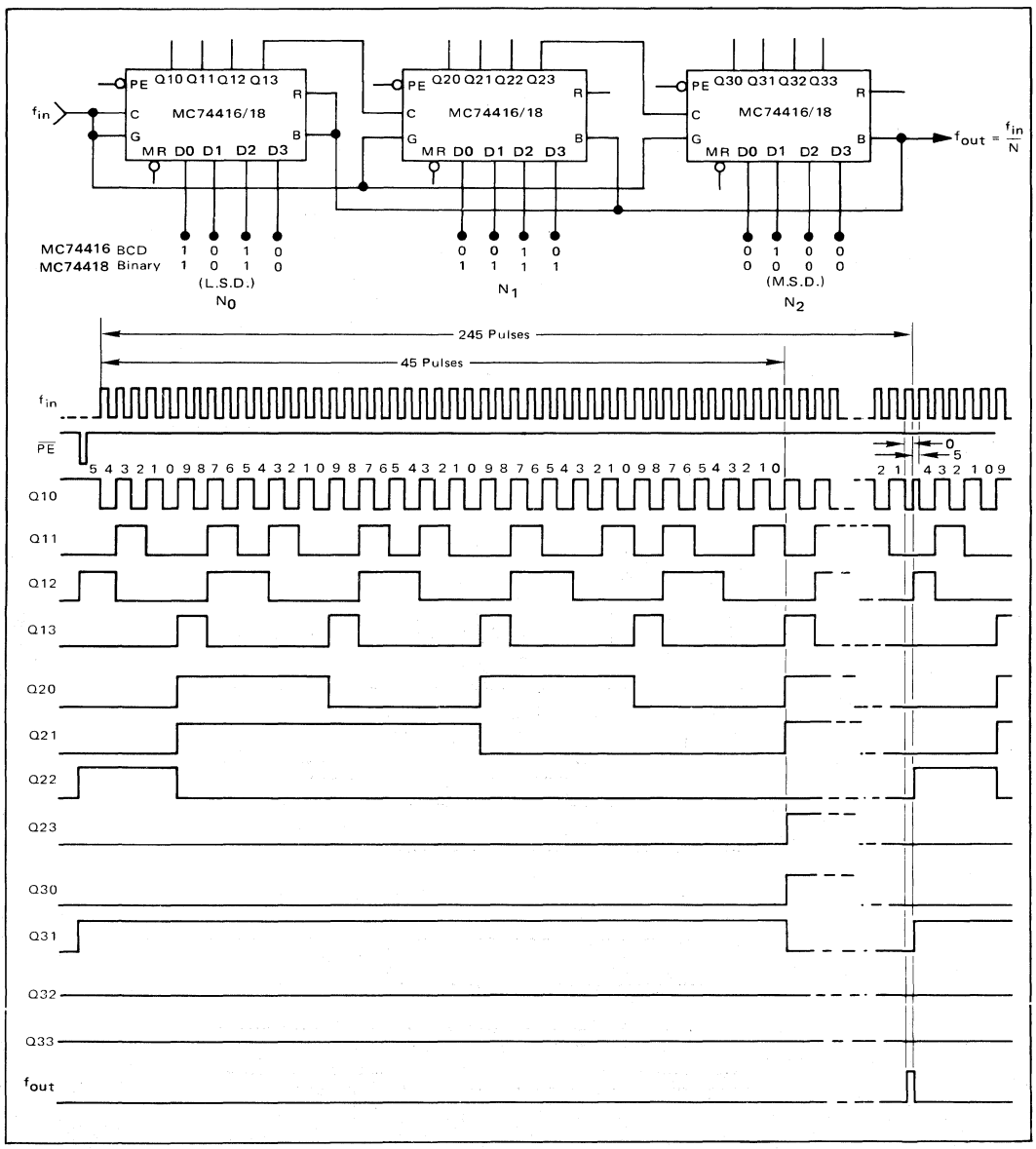
FIGURE 1 – SINGLE-STAGE OPERATION



OPERATING CHARACTERISTICS: MC54416/74416, MC54418/74418 (continued)

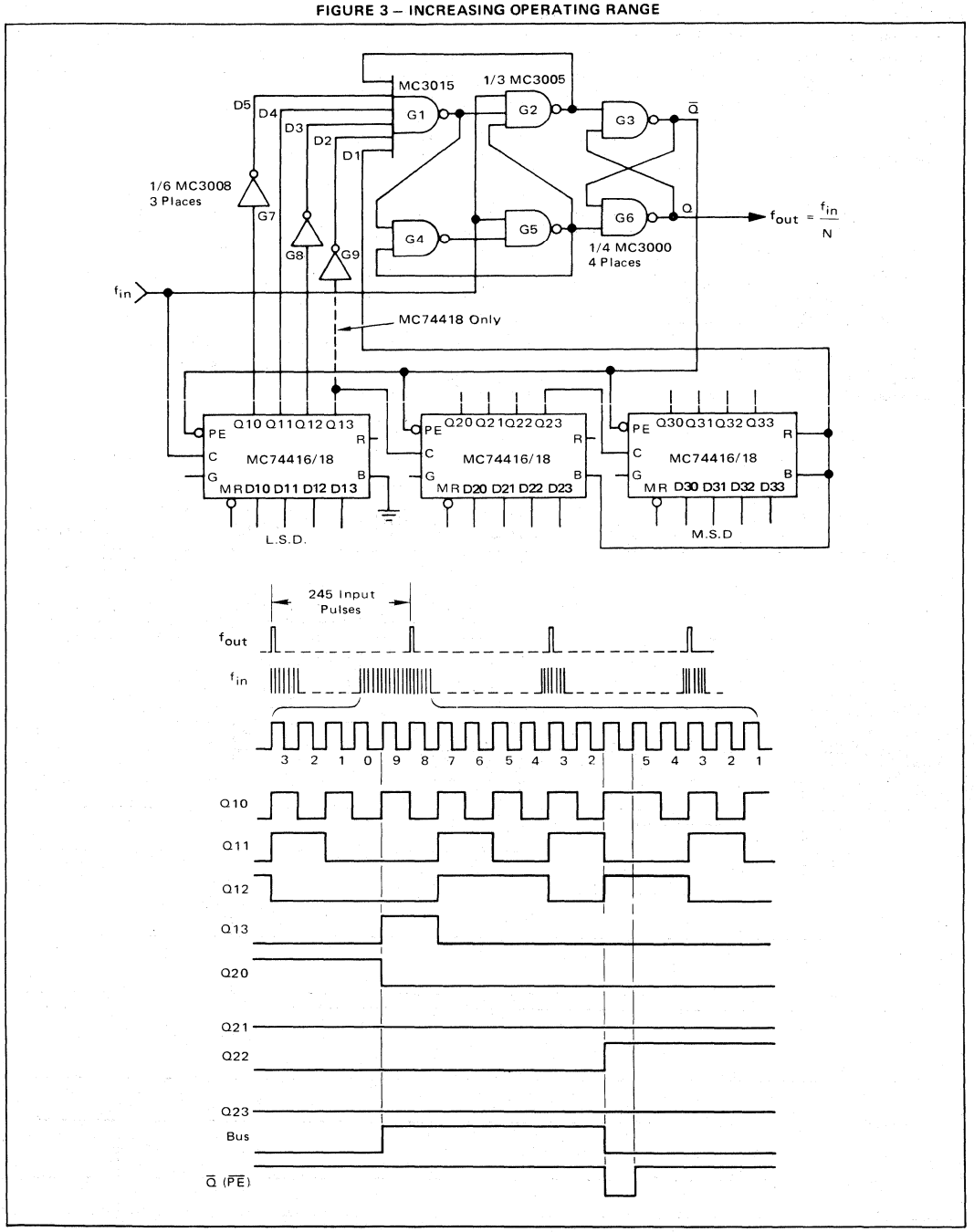
the zero state. Since no reset occurs, the next positive clock edge advances the least significant stage to the nine (1001) state, causing the second stage to be decremented. The process continues in this manner with the least significant stage now dividing by ten. The second stage eventually counts down to zero and also reverts to dividing by ten. Each pulse out of the second stage decrements the third until it reaches zero. At this time the bus line goes high; it remains high until the clock goes low, causing all three stages to be reset to the programmed count again.

FIGURE 2 – CASCADED OPERATION



OPERATING CHARACTERISTICS: MC54416/74416, MC54418/74418 (continued)

FIGURE 3 – INCREASING OPERATING RANGE



5

OPERATING CHARACTERISTICS: MC54416/74416, MC54418/74418 (continued)

Maximum operating frequency of the basic MC74416/74418 counter is limited by the time required for reprogramming at the end of each count down cycle. Operation can be extended to approximately 25 MHz by adding an "early decode" feature as shown in Figure 3. The appropriate connections for three stages are shown; however up to eight stages can be satisfactorily cascaded. Note the following differences between this and the non-extended method: the counter gate inputs are not connected to the input clock; all Parallel Enables are connected to the $\overline{Q}$ output of a type D flip-flop formed by gates G1 through G6; the bus terminal of the least significant stage is grounded; all other bus terminals and one internal resistor, R, are connected together and serve as a data input to the flip-flop. Four additional data inputs are provided for decoding the "two" state of the least significant stage. Circuit operation is illustrated in the waveforms of Figure 3 where the timing for the end of a count-down cycle is shown in expanded form. The counter parallel inputs are assumed to have N = 245 applied. Timing is not shown for the third stage since it has already been counted down to the all zero state. As the next-to-least significant stage reaches zero, the common bus line goes high. Count down of the least significant stage continues until the "two" state is reached. This condition causes the remaining D inputs to the flip-flop to be high. The next-to-last clock pulse of the cycle then triggers the flip-flop Q output high. $\overline{Q}$ simultaneously takes the parallel enable of all stages low, resetting the programmed data to the outputs. The next input pulse clocks Q (f_{out}) back to the zero state, since the data inputs to the flip-flop are no longer all high. The positive output pulse is one input clock period in duration. Note that division by N equal to 1 or 2 is not available using this method.

OPERATING CHARACTERISTICS
MC54417/74417, MC54419/74419

The MC54417/74417 consists of a modulo 2 and a modulo 5 programmable counter. The MC54419/74419 contains two modulo 4 programmable counters. Both parts are implemented in the same manner as the MC54416/MC74416 and MC54418/74418, however in these devices the output of the appropriate flip-flop is disconnected from the input of the next flip-flop. This input is then brought out as the second clock input for the package (see the logic diagrams on page 2 of this data sheet). The resistor existing on the MC54416/74416 and MC54418/74418 is eliminated on the MC54417/74417 and MC54419/74419 in order not to exceed 16 pins. Elimination of the resistor causes no problems because only one resistor is required per divider chain and these parts will normally be used with the MC54416/74416 and/or MC54418/74418. In applications where the parts are used alone, an external resistor is connected to the bus output.

To operate the MC54417/74417 as a modulo 2 programmable counter, the modulo 5 programmable counter must be disabled by programming it to zero (D1, D2, and D3 grounded). Likewise, to use the device as a modulo 5 programmable counter the modulo 2 counter must be disabled (D0 grounded). Operation of the MC54419/74419 is similar in that the modulo 4 counter not being used must be disabled by programming it to zero (D0 and D1 grounded or D2 and D3 grounded).

When cascading packages for large divide ratios, the most significant Q output of the modulo counter being used provides the input for the next package and all bus outputs are tied together. This method of connection is the same as for the MC54416/74416 and MC54418/74418.

The MC54417/74417 and MC54419/74419 can be made to perform the same function as the MC54416/74416 and MC54418/74418 respectively by externally connecting the last Q output of one counter to the clock input of the other counter and programming inputs in the normal manner.

APPLICATIONS INFORMATION

A typical system application for programmable counters is illustrated in the frequency synthesizer shown in Figure 4. There the counter provides a means of digitally selecting some integral multiple of a stable reference frequency. The circuit phase locks the output, f_{VCO}, of a voltage controlled oscillator to a reference frequency, f_{ref}.[1] Circuit operation is such that $f_{VCO} = Nf_{ref}$, where N is the divider ratio of the feedback counter.

In many synthesizer applications the VCO is operated at VHF frequencies too high for direct division by TTL counters. In these cases the VCO output is usually prescaled by using a suitable fixed divide-by-M ECL circuit as shown in Figure 5. For this configuration, $f_{VCO} = NMf_{ref}$, where N is variable (programmable) and M is fixed. Design of the optimum loop filter requires that the input reference frequency be as high as possible where

FIGURE 4 – MTTL PHASE-LOCKED LOOP

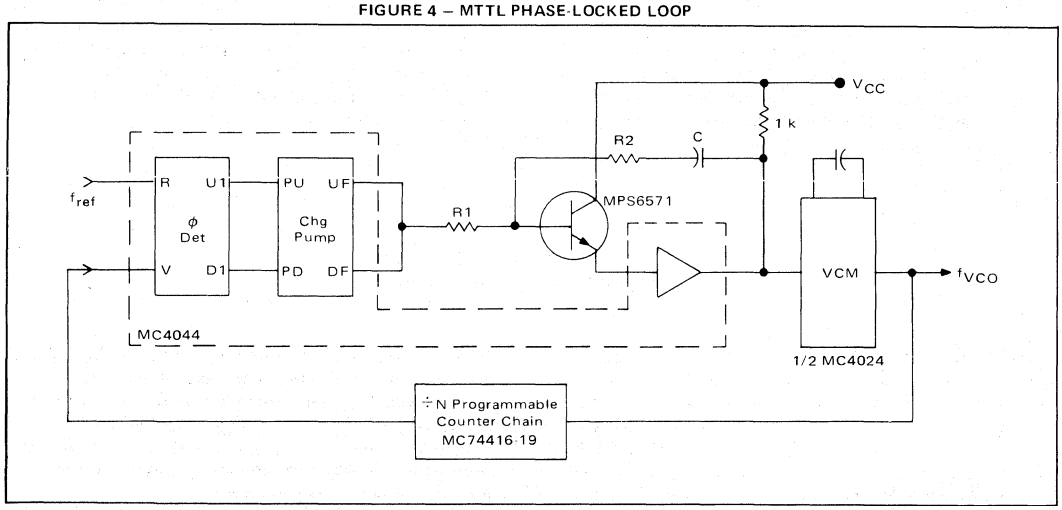
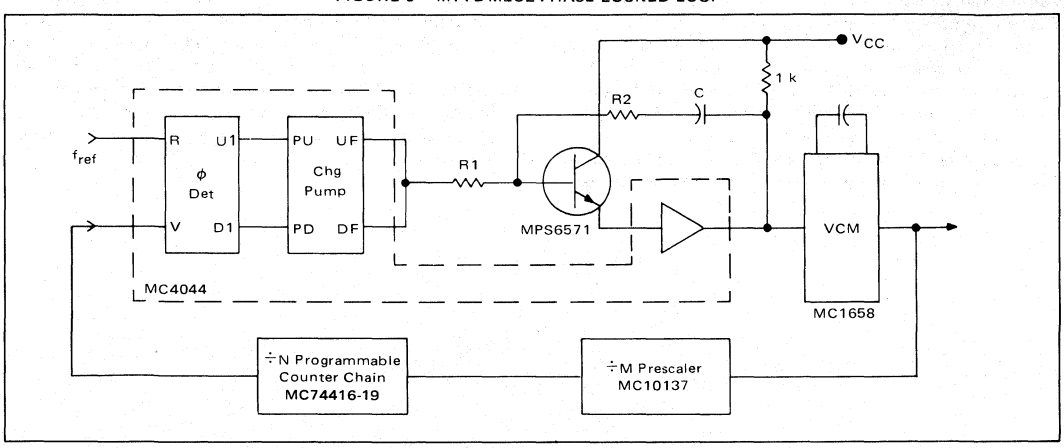
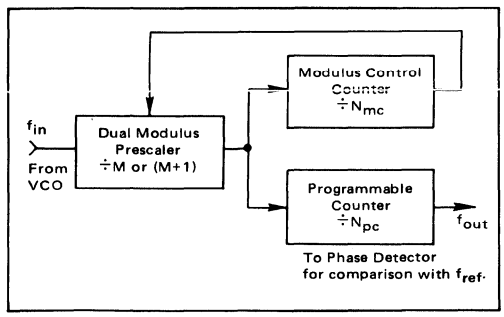


FIGURE 5 – MTTL-MECL PHASE-LOCKED LOOP



1 See Motorola Application Notes AN-535, AN-532, and the MC4344/4044 Data Sheet for detailed explanation of over-all circuit operation.

FIGURE 6 – FEEDBACK COUNTERS WITH DUAL MODULUS PRESCALER



the upper limit is established by the required channel spacing. Since $f_{VCO} = Nf_{ref}$ in the non-prescaled case, if N is changed by one, the VCO output changes by f_{ref}, or the synthesizer channel spacing is just equal to f_{ref}. When the prescaler is used as in Figure 5, $f_{VCO} = NMf_{ref}$, and a change of one in N results in the VCO changing by Mf_{ref}, i.e., if f_{ref} is set equal to the minimum permissible channel spacing as is desirable, then only every M channels in a given band can be selected. One solution is to set f_{ref} = channel spacing/M but this leads to more stringent loop filter requirements.

An alternate approach that avoids this problem is provided by the counter configuration shown in Figure 6.[2] It too uses a prescaler ahead of a programmable counter, however the modulus of the prescaler is now controlled by a third counter, causing it to alternate between M and M + 1. Operation is best explained by assuming that all three counters have been set for the beginning of a cycle: the prescaler for division by (M + 1), the modulus control counter for division by N_{mc}, and the programmable counter for division by N_{pc}. The prescaler will divide by (M + 1) until the modulus control counter has counted down to zero; at this time, the all zero state is detected and causes the prescaler to divide by M until the programmable counter has also counted down to zero. When this occurs, a cycle is complete and each counter is reset to its original modulus in readiness for the next cycle. For this configuration,

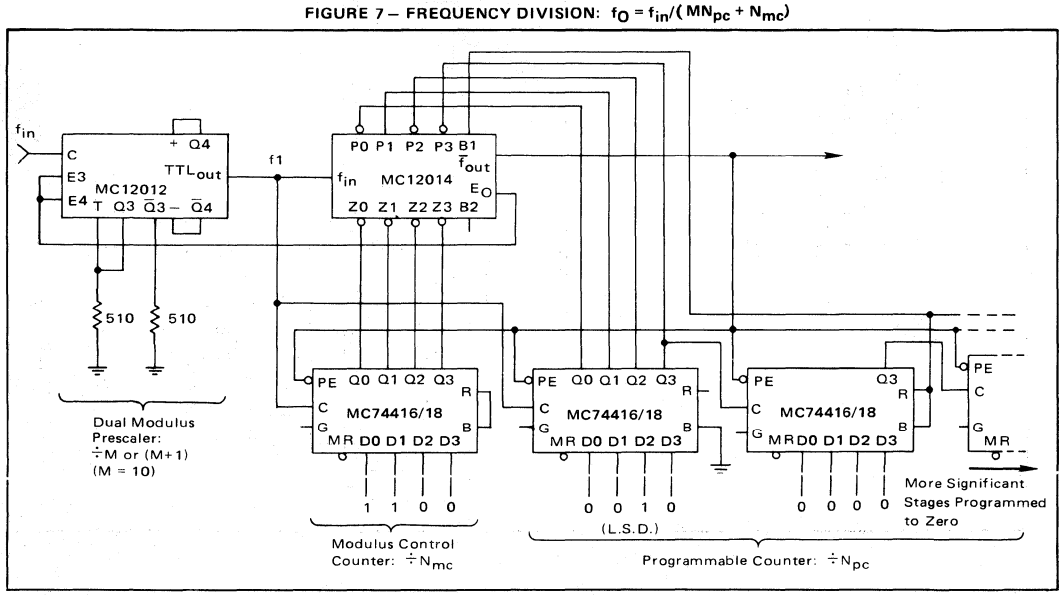
$$f_{out} = \frac{f_{in}}{MN_{pc}+N_{mc}}$$

In terms of the synthesizer application, $f_{VCO} = (MN_{pc} + N_{mc})f_{ref}$ and channels can be selected every f_{ref} by letting N_{pc} and N_{mc} take on suitable integer values, including zero.

A simplified example of this technique is shown in Figure 7. The MC12012 Dual Modulus Prescaler divides by either 10 or 11 when connected as shown in Figure 7. If the E3 and E4 Enable inputs are high at the start of a prescaler cycle, division by 10 results; if the Enable inputs are low at the beginning of the cycle, division by 11 results. The zero detection circuitry of the MC12014 Counter Control Logic is connected to monitor the outputs of the modulus control counter; this provides a suitable enable signal at E0 as the modulus control counter reaches its terminal (zero) count. The remainder of the MC12014 is connected to extend the operating frequency of the programmable counter chain.

A specific example of this technique is shown in Figure 8. There the feedback divider circuitry required for generating frequencies between 144 MHz and 178 MHz with 30 kHz channel spacing is shown.[2]

FIGURE 7 – FREQUENCY DIVISION: $f_O = f_{in}/(MN_{pc} + N_{mc})$



2. This application is discussed in greater detail in the MC12014 Counter Control Logic data sheet.

FIGURE 8 – 144 TO 178 MHz FREQUENCY SYNTHESIZER WITH 30 kHz CHANNEL SPACING

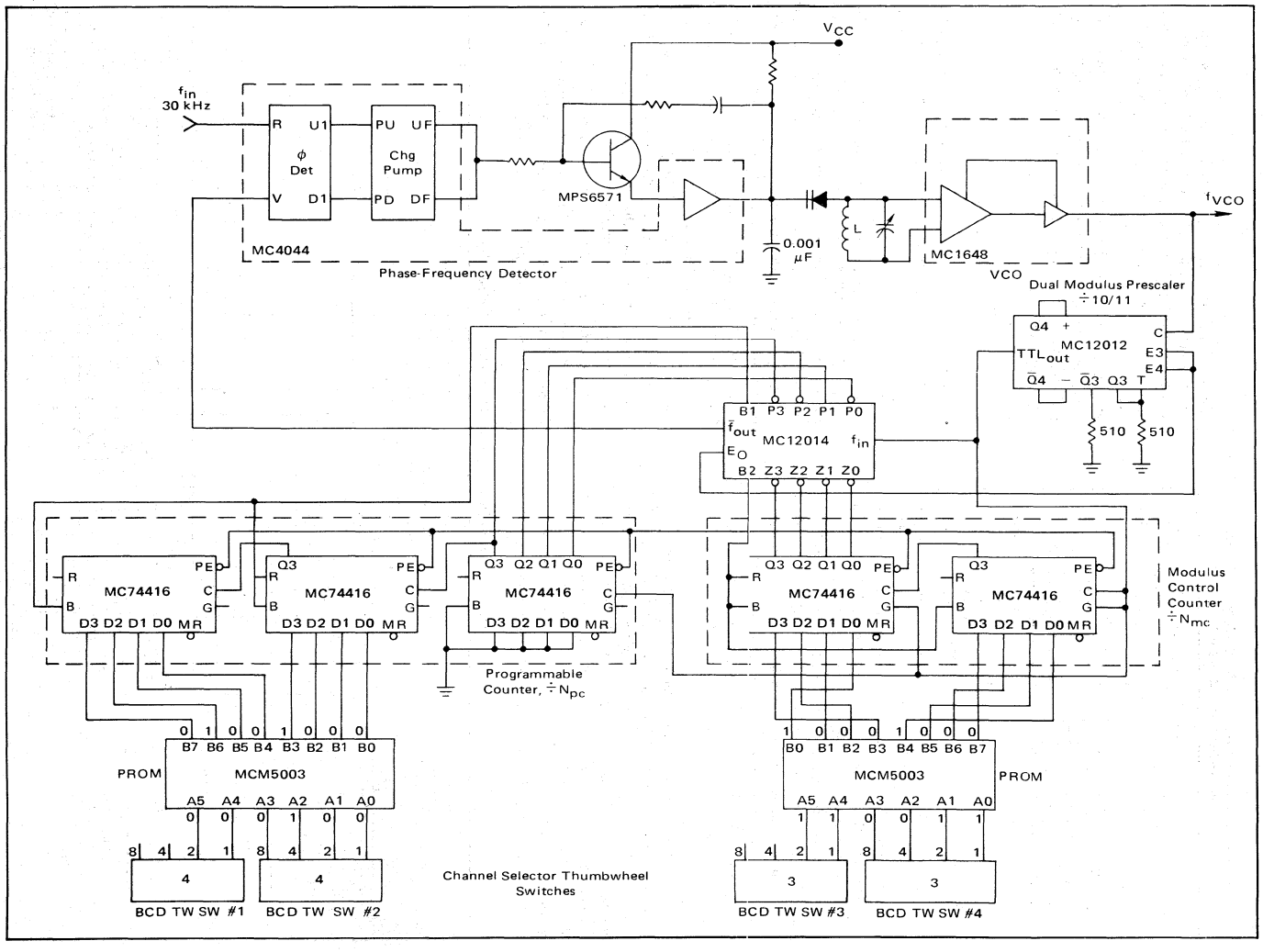


Figure 9 shows a frequency synthesizer system for the aircraft band of 108 to 136 MHz, with a channel spacing of 50 kHz. The use of the MC74417 as a modulo 2 programmable counter is shown in Figure 9A, while Figure 9B shows the same system implemented using the MC74416. For a system of this type it is desirable to use direct-reading thumbwheel switches for channel selection. To implement this system with these constraints, it is necessary to calculate the required reference frequency (f_{ref}). Using the equations in Figure 9A, the required reference is 50 kHz and N4 must be programmed to 0 and 1. Figure 9B requires a reference frequency of 10 kHz and N4 must be programmed to only 0 and 5.

For any phase-locked loop system it is desirable to maintain as high a reference frequency as possible while meeting the system requirements. The higher the reference frequency, the higher the number of sampling pulses received by the phase detector per unit time. This results in (1) easier filtering of the control voltage, (2) faster lock-up time, and (3) less noise in the output spectrum. The higher reference frequency is also desirable because the reference frequency appears as sidebands on the output frequency and the farther the sidebands are away from the output the better the system. Another advantage of the higher reference frequency is the smaller divide ratio required in the programmable counter chain. This is advantageous when calculating realizable resistors for the filter. For these reasons, the system using the MC74417 is superior to the one using the MC74416.

FIGURE 9 – 108 TO 136 MHz FREQUENCY SYNTHESIZER WITH 50 kHz CHANNEL SPACING

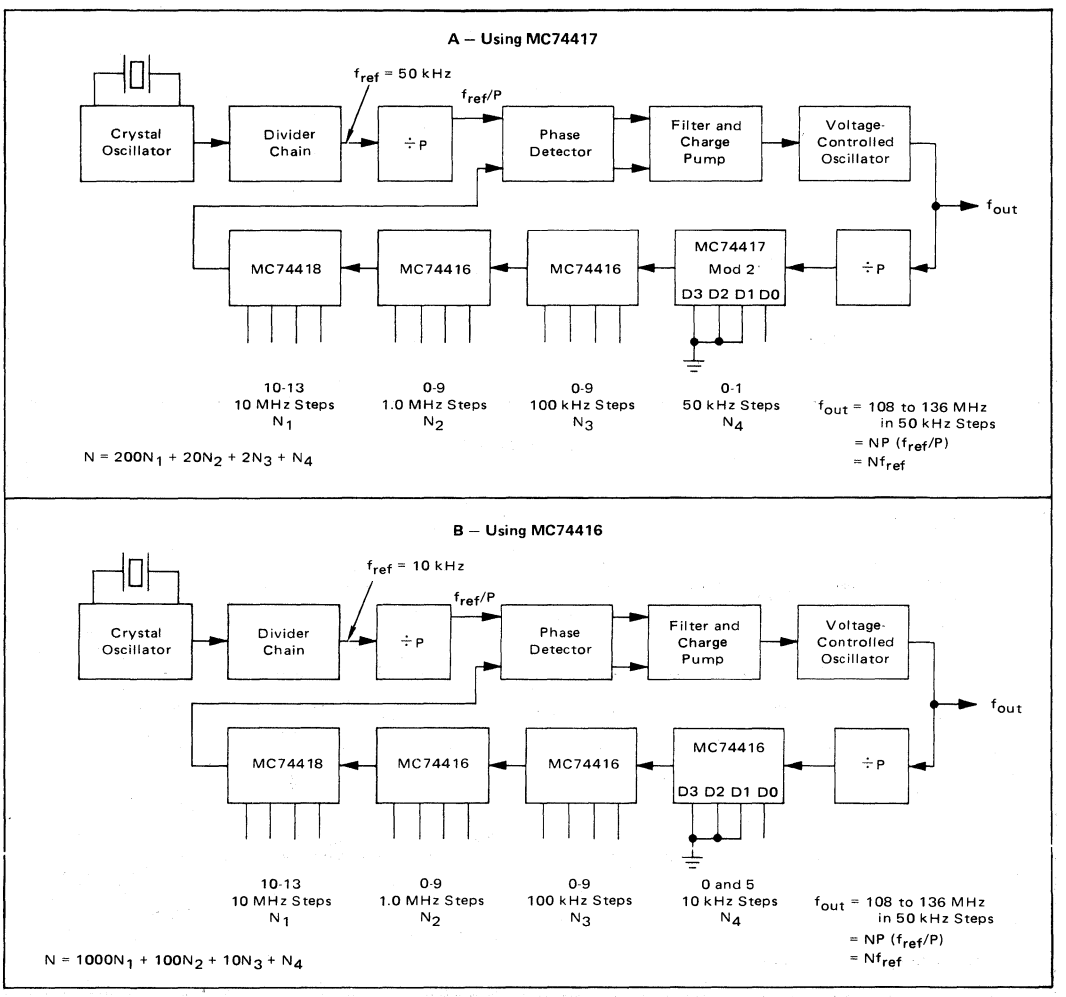
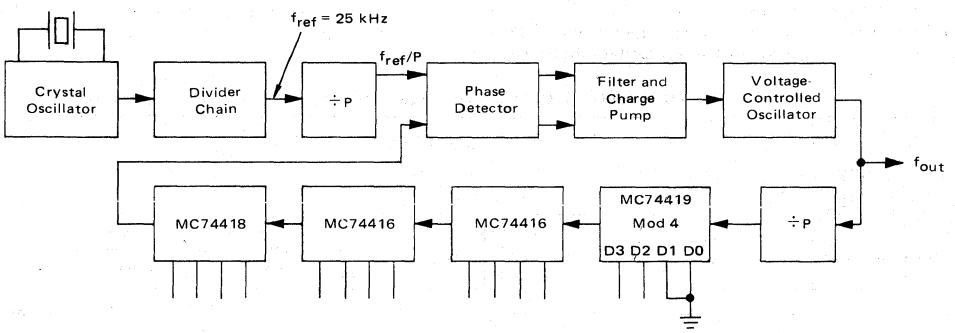


Figure 10 shows the implementation of the aircraft band synthesizer with 25 kHz channel spacing (the 25 kHz spacing has been proposed to the FCC). The system is implemented in Figure 10A using the MC74419, and has a reference frequency of 25 kHz. Figure 10B shows the system using an MC74418 as the first counter, and has a reference frequency of 6.25 kHz to obtain the direct programming.

FIGURE 10 – 108 TO 136 MHz FREQUENCY SYNTHESIZER WITH 25 kHz CHANNEL SPACING

A – Using MC74419



10-13
10 MHz Steps
N_1

0-9
1.0 MHz Steps
N_2

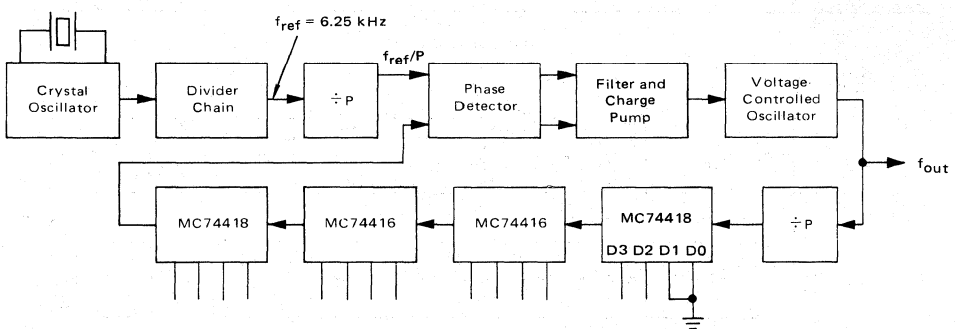
0-9
100 kHz Steps
N_3

0-4
25 kHz Steps
N_4

f_{out} = 108 to 136 MHz in 25 kHz Steps
= NP (f_{ref}/P)
= Nf_{ref}

$N = 400N_1 + 40N_2 + 4N_3 + N_4$

B – Using MC74418



10-13
6.25 MHz Steps
N_1

0-9
625 kHz Steps
N_2

0-9
62.5 kHz Steps
N_3

0,4,8,12
6.25 kHz Steps
N_4

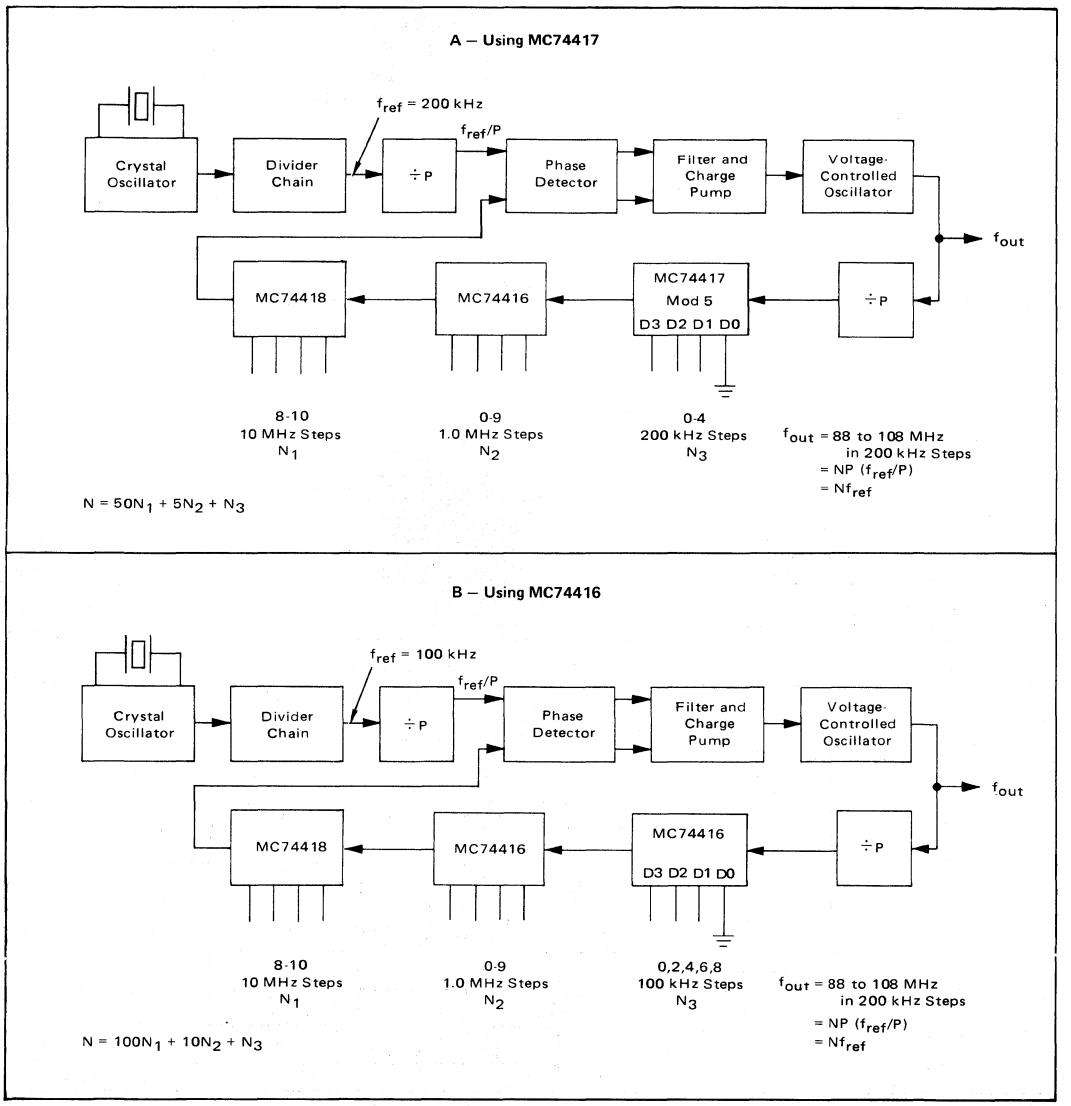
f_{out} = 108 to 136 MHz in 25 kHz Steps
= NP (f_{ref}/P)
= Nf_{ref}

$N = 1600N_1 + 160N_2 + 16N_3 + N_4$

Figures 11A and 11B show the FM band implemented with MC74417 (used as a modulo 5 counter) and MC-74416 respecitvely. The first system has a 200 kHz reference frequency, and the second system has a 100 kHz reference frequency. These systems using the MC74417/19 offer the same advantages over the MC74416/18 as with the aircraft band systems.

These examples illustrate the desirability of the MC-54417/74417 for phase-locked loop applications where the channel spacing is 2 x 10^n Hz when used as a modulo 5 programmable counter, and 5 x 10^n Hz when used as a modulo 2 programmable counter. The MC54419/74419 is for applications with a channel spacing of 2.5 x 10^n Hz. The MC54416/74416 covers phase-locked loop applications where the channel spacing is 1 x 10^n Hz. The MC54418/74418 is used when the most significant digit is between 9 and 15.

FIGURE 11 – 88 TO 108 MHz FREQUENCY SYNTHESIZER WITH 200 kHz CHANNEL SPACING



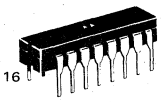
5

TWO-MODULUS PRESCALER

MC12012

The MC12012 is a two-modulus prescaler which consists of three functional blocks: 1) a controllable divide by 5/divide by 6 prescaler; 2) a divide by 2 prescaler; and 3) a MECL to MTTL translator. When used with the MC12014 Counter Control Logic function and the MC4016 programmable counter, a divide by N programmable counter can be constructed for operation to 200 MHz. This arrangement is especially useful in frequency synthesizer applications.

- ÷2, ÷5/÷6, ÷10/÷11, ÷10/÷12
- MECL to MTTL Translator on Chip
- +5.0 or -5.2 V operation
- 200 MHz (typ) Toggle Frequency



CERAMIC PACKAGE
CASE 620

PIN ASSIGNMENT

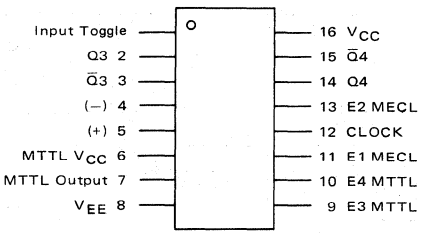
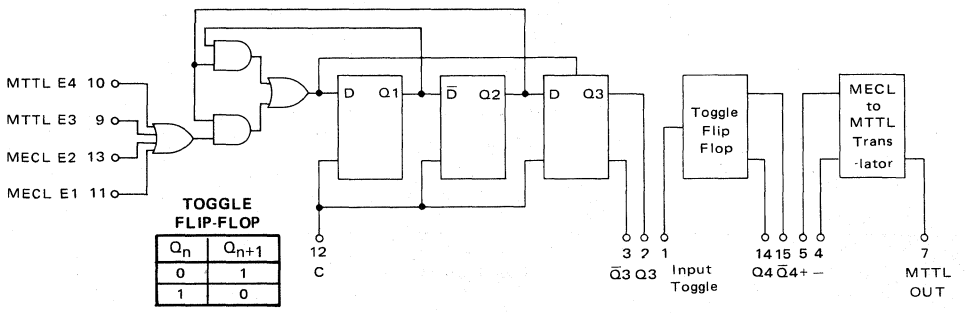


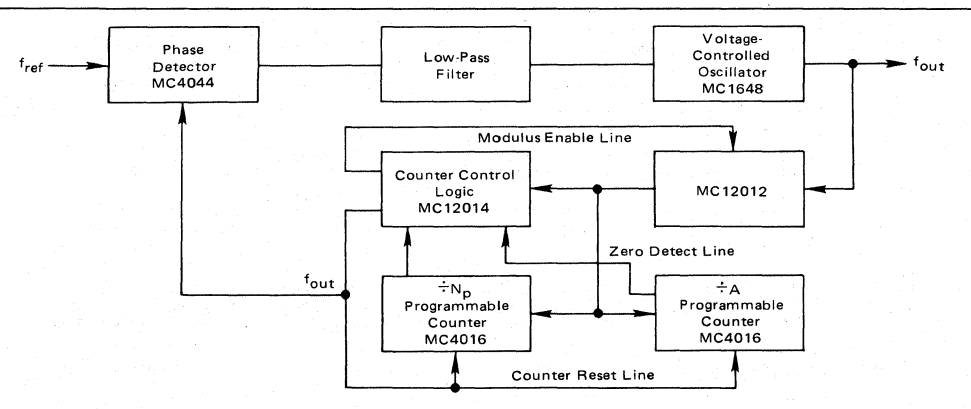
FIGURE 1 – LOGIC DIAGRAM



TOGGLE FLIP-FLOP

Q_n	Q_{n+1}
0	1
1	0

FIGURE 2 – TYPICAL FREQUENCY SYNTHESIZER APPLICATION



ELECTRICAL CHARACTERISTICS

Supply Voltage -5.2 V

Characteristic	Symbol	Rating	Unit
Ratings above which device life may be impaired:			
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8.0	Vdc
Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{IL} min	Vdc
Output Source Current	I_o	20	mAdc
Storage Temperature Range	T_{stg}	-55 to +125	°C
Recommended maximum ratings above which performance may be degraded:			
Operating Temperature Range	T_A	0 to +75	°C
DC Fan-Out* (Gates and Flip-Flops)	n	70	–

*AC fan-out is limited by desired system performance.

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{IHT}	V_{ILT}	V_{EE}	(mA) I_L	I_{OL}	I_{OH}
0°C	-0.840	-1.870	-1.145	-1.490	-4.7	-2.8	+0.3	-0.7	-3.2	-4.4	-5.2	-2.5	16	-1.6
25°C	-0.810	-1.850	-1.105	-1.475	-4.7	-2.8	+0.3	-0.7	-3.2	-4.4	-5.2	-2.5	16	-1.6
75°C	-0.720	-1.880	-1.045	-1.450	-4.7	-2.8	+0.3	-0.7	-3.2	-4.4	-5.2	-2.5	16	-1.6

Characteristic	Symbol	Pin Under Test	MC12012 0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{IHT}	V_{ILT}	V_{EE}	I_L	I_{OL}	I_{OH}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	100	–	–	–	mAdc	–	–	–	–	–	–	–	–	–	–	8	–	–	–	6,16
Input Current	I_{INH1}	12	–	–	–	100	200	–	–	µAdc	12	–	–	–	–	–	–	–	–	–	8	–	–	–	16
	I_{INH2}	1	–	–	–	40	100	–	–	µAdc	1	–	–	–	–	–	–	–	–	–	8	–	–	–	16
		11	–	–	–	40	100	–	–		11	–	–	–	–	–	–	–	–	–	8	–	–	–	16
		13	–	–	–	40	100	–	–		13	–	–	–	–	–	–	–	–	–	8	–	–	–	16
	I_{INH3}	9	–	–	–	–	40	–	–	µAdc	–	–	–	–	–	–	9	–	–	–	8	–	–	–	16
		10	–	–	–	–	40	–	–		–	–	–	–	–	–	10	–	–	–	8	–	–	–	16
	I_{INH4}	4	–	–	3.5	–	5.5	–	–	mAdc	5	4	–	–	–	–	–	–	–	–	8	–	–	–	6
		5	–	–	3.5	–	5.5	–	–	mAdc	5	4	–	–	–	–	–	–	–	–	8	–	–	–	6
	I_{INL1} (Leakage Current)	1	–	–	–	–	2.0	–	–	µAdc	–	–	–	–	–	–	–	–	–	–	1,8	–	–	–	16
		11	–	–	–	–	↓	–	–	↓	–	–	–	–	–	–	–	–	–	–	8,11	–	–	–	↓
		12	–	–	–	–		–	–		–	–	–	–	–	–	–	–	–	–	8,12	–	–	–	
		13	–	–	–	–		–	–		–	–	–	–	–	–	–	–	–	–	8,13	–	–	–	
	I_{INL2}	9	–	–	1.1	–	2.2	–	–	mAdc	–	–	–	–	9	–	–	–	–	–	8	–	–	–	16
		10	–	–	1.1	–	2.2	–	–	mAdc	–	–	–	–	10	–	–	–	–	–	8	–	–	–	16
	I_{INL3}	4	–	–	3.8	–	6.5	–	–	mAdc	4	5	–	–	–	–	–	–	–	–	8	–	–	–	16
		5	–	–	2.0	–	4.0	–	–	mAdc	4	5	–	–	–	–	–	–	–	–	8	–	–	–	16
Logic "1" Output Voltage	V_{OH1} ②	2	-1.000	-0.840	-0.960	–	-0.810	-0.900	-0.720	Vdc	–	11,13	–	–	9,10	–	–	–	–	–	8	2	–	–	16
		3	↓	↓	↓	–	↓	↓	↓	↓	–	11,13	–	–	9,10	–	–	–	–	–		3	–	–	↓
		14				–					–	–	–	–	–	–	–	–	–	–		14	–	–	
		15				–					–	–	–	–	–	–	–	–	–	–	↓	15	–	–	
	V_{OH2}	7	-2.800	–	-2.800	–	–	-2.800	–	Vdc	5	4	–	–	–	–	–	–	–	–	8	–	–	7	6
Logic "0" Output Voltage	V_{OL1} ②	2	-1.870	-1.635	-1.850	–	-1.620	-1.830	-1.595	Vdc	–	11,13	–	–	9,10	–	–	–	–	–	8	2	–	–	16
		3	↓	↓	↓	–	↓	↓	↓	↓	–	11,13	–	–	9,10	–	–	–	–	–		3	–	–	↓
		14				–					–	–	–	–	–	–	–	–	–	–		14	–	–	
		15				–					–	–	–	–	–	–	–	–	–	–	↓	15	–	–	
	V_{OL2}	7	–	-4.700	–	–	-4.700	–	-4.700	Vdc	4	5	–	–	–	–	–	–	–	–	8	–	7	–	6
Logic "1" Threshold Voltage	V_{OHA}	2 ③	-1.020	–	-0.980	–	–	-0.920	–	Vdc	–	–	11,13	–	–	–	–	–	9,10	–	8	2	–	–	16
		3 ③	↓	–	↓	–	–	↓	–	↓	–	–	11,13	–	–	–	–	–	9,10	–		3	–	–	↓
		14 ④		–		–	–		–		–	–	–	–	–	–	–	–	–	–		14	–	–	
		15 ④		–		–	–		–		–	–	–	–	–	–	–	–	–	–	↓	15	–	–	
Logic "0" Threshold Voltage	V_{OLA}	2 ⑤	–	-1.615	–	–	-1.600	–	-1.575	Vdc	–	–	–	11,13	–	–	–	–	–	9,10	8	2	–	–	16
		3 ⑤	–	↓	–	–	↓	–	↓	↓	–	–	–	11,13	–	–	–	–	–	9,10		3	–	–	↓
		14 ④	–		–	–		–			–	–	–	–	–	–	–	–	–	–		14	–	–	
		15 ④	–		–	–		–			–	–	–	–	–	–	–	–	–	–	↓	15	–	–	
Short Circuit Voltage	I_{SC}	7	-20	-65	-20	–	-65	-20	-65	mAdc	5	4	–	–	–	–	–	–	–	–	8	–	–	–	6

ELECTRICAL CHARACTERISTICS

Supply Voltage +5.0 V

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts)											TEST VOLTAGE/CURRENT VALUES (mA)		
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{IHT}	V_{ILT}	V_{CC}	I_L	I_{OL}	I_{OH}
0°C	+4.160	+3.130	+3.855	+3.510	+0.5	+2.4	+5.5	+4.5	+2.0	+0.8	+5.0	-2.5	16	-1.6
25°C	+4.190	+3.150	+3.895	+3.525	+0.5	+2.4	+5.5	+4.5	+2.0	+0.8	+5.0	-2.5	16	-1.6
75°C	+4.280	+3.170	+3.955	+3.550	+0.5	+2.4	+5.5	+4.5	+2.0	+0.8	+5.0	-2.5	16	-1.6

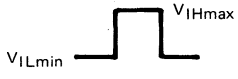
Characteristic	Symbol	Pin Under Test	MC12012 0°C Min	MC12012 0°C Max	MC12012 +25°C Min	MC12012 +25°C Typ	MC12012 +25°C Max	MC12012 +75°C Min	MC12012 +75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{IHT}	V_{ILT}	V_{CC}	I_L	I_{OL}	I_{OH}	(V_{EE}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	95	–	–	–	mAdc	–	–	–	–	–	–	–	–	–	–	6,16	–	–	–	8
Input Current	I_{INH1}	12	–	–	–	100	200	–	–	µAdc	12	–	–	–	–	–	–	–	–	–	16	–	–	–	8
	I_{INH2}	1	–	–	–	40	100	–	–	µAdc	1	–	–	–	–	–	–	–	–	–	16	–	–	–	8
		11	–	–	–	40	100	–	–		11	–	–	–	–	–	–	–	–	–	16	–	–	–	8
		13	–	–	–	40	100	–	–		13	–	–	–	–	–	–	–	–	–	16	–	–	–	8
	I_{INH3}	9	–	–	–	–	40	–	–	µAdc	–	–	–	–	–	–	9	–	–	–	16	–	–	–	8
		10	–	–	–	–	40	–	–		–	–	–	–	–	–	10	–	–	–	16	–	–	–	8
	I_{INH4}	4	–	–	3.5	–	5.5	–	–	mAdc	5	4	–	–	–	–	–	–	–	–	6	–	–	–	8
		5	–	–	3.5	–	5.5	–	–	mAdc	5	4	–	–	–	–	–	–	–	–	6	–	–	–	8
	I_{INL1} (Leakage Current)	1	–	–	–	–	2.0	–	–	µAdc	–	–	–	–	–	–	–	–	–	–	16	–	–	–	1,8
		11	–	–	–	–	↓	–	–		–	–	–	–	–	–	–	–	–	–	↓	–	–	–	8,11
		12	–	–	–	–		–	–		–	–	–	–	–	–	–	–	–	–		–	–	–	8,12
		13	–	–	–	–		–	–		–	–	–	–	–	–	–	–	–	–		–	–	–	8,13
	I_{INL2}	9	–	–	1.1	–	2.2	–	–	mAdc	–	–	–	–	9	–	–	–	–	–	16	–	–	–	8
		10	–	–	1.1	–	2.2	–	–	mAdc	–	–	–	–	10	–	–	–	–	–	16	–	–	–	8
	I_{INL3}	4	–	–	3.8	–	6.5	–	–	mAdc	4	5	–	–	–	–	–	–	–	–	6	–	–	–	8
		5	–	–	2.0	–	4.0	–	–	mAdc	4	5	–	–	–	–	–	–	–	–	6	–	–	–	8
Logic "1" Output Voltage ②	V_{OH1}	2	4.000	4.160	4.040	–	4.190	4.100	4.280	Vdc	–	11,13	–	–	9,10	–	–	–	–	–	16	2	–	–	8
		3	↓	↓	↓	–	↓	↓	↓	↓	–	11,13	–	–	9,10	–	–	–	–	–	↓	3	–	–	↓
		14				–					–	–	–	–	–	–	–	–	–	–		14	–	–	
		15				–					–	–	–	–	–	–	–	–	–	–		15	–	–	
	V_{OH2}	7	2.400	–	2.400	–	–	2.400	–	Vdc	5	4	–	–	–	–	–	–	–	–	6	–	–	7	8
Logic "0" Output Voltage ②	V_{OL1}	2	3.130	3.370	3.150	–	3.380	3.170	3.410	Vdc	–	11,13	–	–	9,10	–	–	–	–	–	16	2	–	–	8
		3	↓	↓	↓	–	↓	↓	↓	↓	–	11,13	–	–	9,10	–	–	–	–	–	↓	3	–	–	↓
		14				–					–	–	–	–	–	–	–	–	–	–		14	–	–	
		15				–					–	–	–	–	–	–	–	–	–	–		15	–	–	
	V_{OL2}	7	–	0.500	–	–	0.500	–	0.500	Vdc	4	5	–	–	–	–	–	–	–	–	6	–	7	–	8
Logic "1" Threshold Voltage	V_{OHA}	2 ③	3.980	–	4.020	–	–	4.080	–	Vdc	–	–	11,13	–	–	–	–	–	9,10	–	16	2	–	–	8
		3 ③	↓	–	↓	–	–	↓	–	↓	–	–	11,13	–	–	–	–	–	9,10	–	↓	3	–	–	↓
		14 ④		–		–	–		–		–	–	–	–	–	–	–	–	–	–		14	–	–	
		15 ④		–		–	–		–		–	–	–	–	–	–	–	–	–	–		15	–	–	
Logic "0" Threshold Voltage	V_{OLA}	2 ⑤	–	3.390	–	–	3.400	–	3.430	Vdc	–	–	–	11,13	–	–	–	–	–	9,10	16	2	–	–	8
		3 ⑤	–	↓	–	–	↓	–	↓	↓	–	–	–	11,13	–	–	–	–	–	9,10	↓	3	–	–	↓
		14 ④	–		–	–		–			–	–	–	–	–	–	–	–	–	–		14	–	–	
		15 ④	–		–	–		–			–	–	–	–	–	–	–	–	–	–		15	–	–	
Short Circuit Voltage	I_{SC}	7	-20	-65	-20	–	-65	-20	-65	mAdc	5	4	–	–	–	–	–	–	–	–	6	–	–	–	8

Characteristic	Symbol	Pin Under Test	MC12012 0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW: Pulse Gen. 1	Pulse Gen. 2	Pulse Gen. 3	V_{IHmin} +1.100	V_{ILmin} +0.130	V_R +0.000	V_F -3.0 V	V_{EE} -3.0 or -3.2	V_{CC} +2.0
Propagation Delay (See Figures 3 and 4)	t_{12+2+}	12,2	–	–	2.0	3.0	4.0	–	–	ns	12	–	–	–	11,13	–	9,10	8	6,16
	t_{12+3+}	12,3	–	–	↓	3.0	↓	–	–	↓	–	–	–	–	11,13	–	9,10	↓	↓
	t_{12+}	12,2	–	–	↓	2.8	↓	–	–	↓	–	–	–	–	11,13	–	9,10	↓	↓
	t_{12+3-}	12,3	–	–	↓	2.8	↓	–	–	↓	–	–	–	–	11,13	–	9,10	↓	↓
	t_{1+14+}	1,14	–	–	↓	3.0	↓	–	–	↓	1	–	–	–	–	–	–	↓	↓
	t_{1+15+}	1,15	–	–	↓	3.0	↓	–	–	↓	↓	–	–	–	–	–	–	↓	↓
	t_{1+14-}	1,14	–	–	↓	2.8	↓	–	–	↓	↓	–	–	–	–	–	–	↓	↓
	t_{1+15-}	1,15	–	–	↓	2.8	↓	–	–	↓	↓	–	–	–	–	–	–	↓	↓
	t_{5+7+}	5,7	–	–	↓	8.0	12.0	–	–	↓	A	–	–	–	–	–	–	↓	↓
	t_{5-7-}	5,7	–	–	↓	5.0	10.0	–	–	↓	A	–	–	–	–	–	–	↓	↓
Output Rise Time (See Figure 4)	t_{2+}	2	–	–	–	2.0	–	–	–	ns	12	–	–	–	11,13	–	9,10	8	6,16
	t_{3+}	3	–	–	–	2.0	–	–	–	↓	12	–	–	–	11,13	–	9,10	↓	↓
	t_{14+}	14	–	–	–	2.0	–	–	–	↓	1	–	–	–	–	–	–	↓	↓
	t_{15+}	15	–	–	–	2.0	–	–	–	↓	1	–	–	–	–	–	–	↓	↓
Output Fall Time (See Figure 4)	t_{2-}	2	–	–	–	2.0	–	–	–	ns	12	–	–	–	11,13	–	9,10	8	6,16
	t_{3-}	3	–	–	–	2.0	–	–	–	↓	12	–	–	–	11,13	–	9,10	↓	↓
	t_{14-}	14	–	–	–	2.0	–	–	–	↓	1	–	–	–	–	–	–	↓	↓
	t_{15-}	15	–	–	–	2.0	–	–	–	↓	1	–	–	–	–	–	–	↓	↓
Setup Time (See Figure 5)	t_{setup1}	11,13	–	4.0	–	2.4	3.0	–	4.0	ns	12	11/13	–	–	13/11	–	9,10	8	6,16
	t_{setup2}	9,10	–	7.0	–	5.0	7.0	–	8.5	ns	12	–	9/10	–	11,13	–	10/9	8	6,16
Release Time (See Figure 5)	t_{rel1}	11,13	–	2.5	–	1.2	2.0	–	2.0	ns	12	11/13	–	–	13/11	–	9,10	8	6,16
	t_{rel2}	9,10	–	4.0	–	2.5	3.5	–	2.0	ns	12	–	9/10	–	11,13	–	10/9	8	6,16
Toggle Frequency	f_{max}									MHz									
Figure 6 (÷5)	↓	2	–	–	175	200	–	–	–	↓	–	–	–	11	13	–	9,10	8	16
(÷6)	↓	2	–	–	↓	↓	–	–	–	↓	–	–	–	–	11,13	–	9,10	↓	↓
(÷2)	↓	14	–	–	↓	↓	–	–	–	↓	–	–	–	–	–	–	–	↓	↓
Figure 7 (÷10 or 11)	↓	14	–	–	↓	↓	–	–	–	↓	–	–	–	–	–	–	–	↓	↓

① All MECL outputs (2,3,14,15) are terminated to V_{EE} through an external 510 Ω resistor during the DC tests.

② Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests. The clock input is

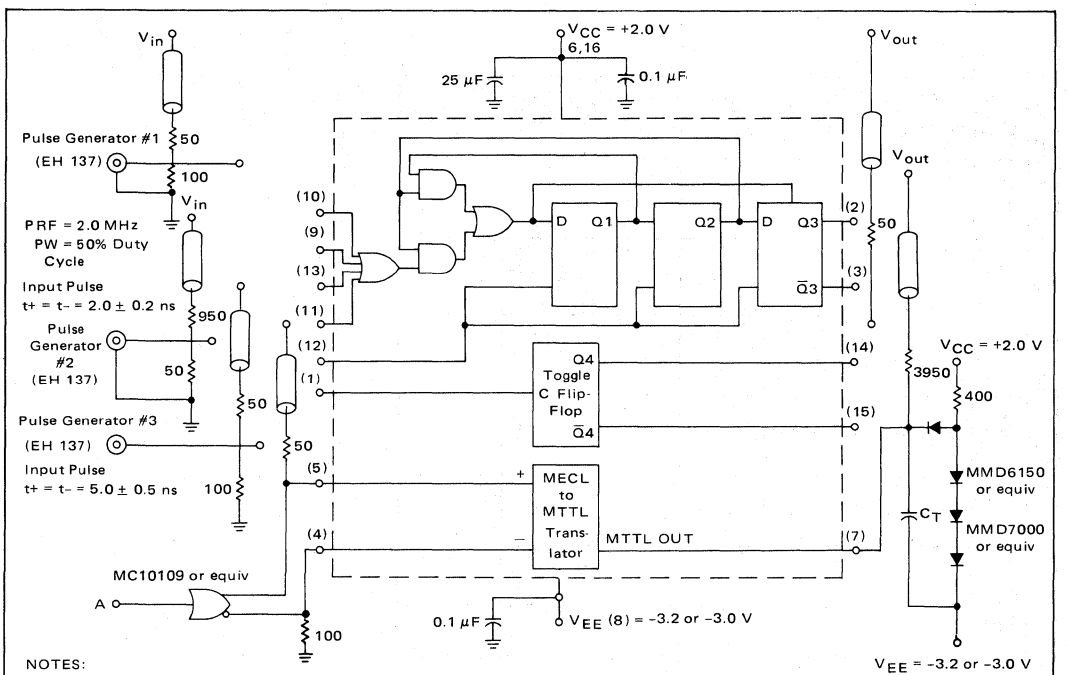
③ In addition to meeting the output levels specified, the device must divide by 5 during this test. The clock input is



④ In addition to meeting the output levels specified the device must divide by 2 with a clock input of

⑤ In addition to meeting the output levels specified, the device must divide by 6 during this test. The clock input is

FIGURE 3 – AC TEST CIRCUIT



NOTES:

All input and output cables to the scope are equal lengths of 50 Ω coaxial cable.

All unused cables must be terminated with 50 ohms.

All resistors are + 1%.

C_T = 15 pF = total parasitic capacitance which includes probe, wiring, and load capacitance.

The 950-ohm resistor and the scope termination impedance constitute a 20:a attenuator probe.

The 50-ohm resistor and the scope termination impedance constitute a 2:1 attenuator probe.

FIGURE 4 – AC VOLTAGE WAVEFORMS

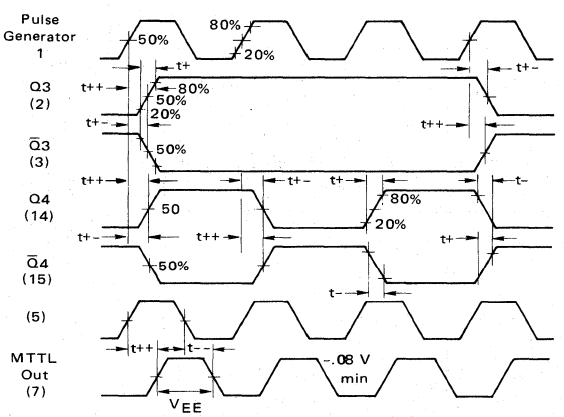


FIGURE 5 – SETUP AND RELEASE TIME WAVEFORMS

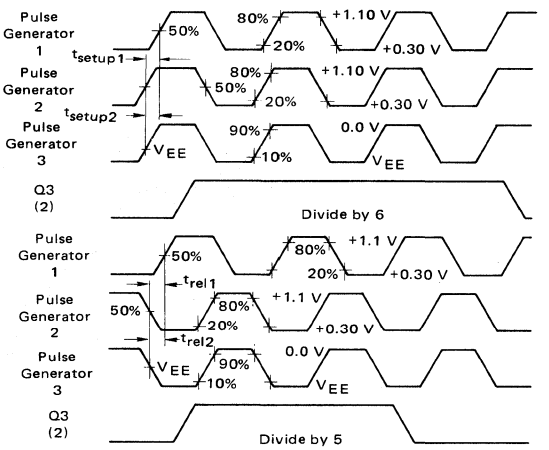
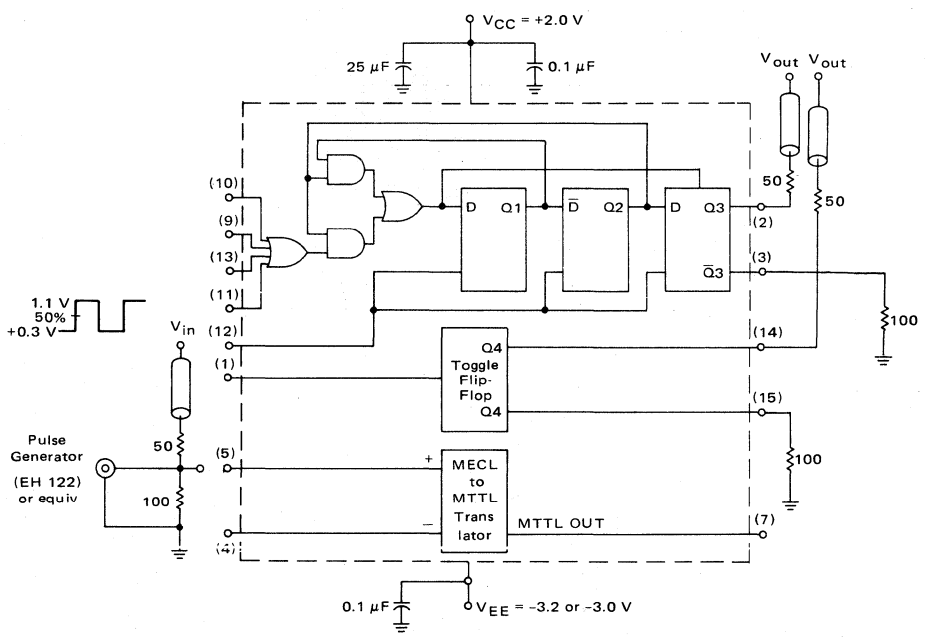
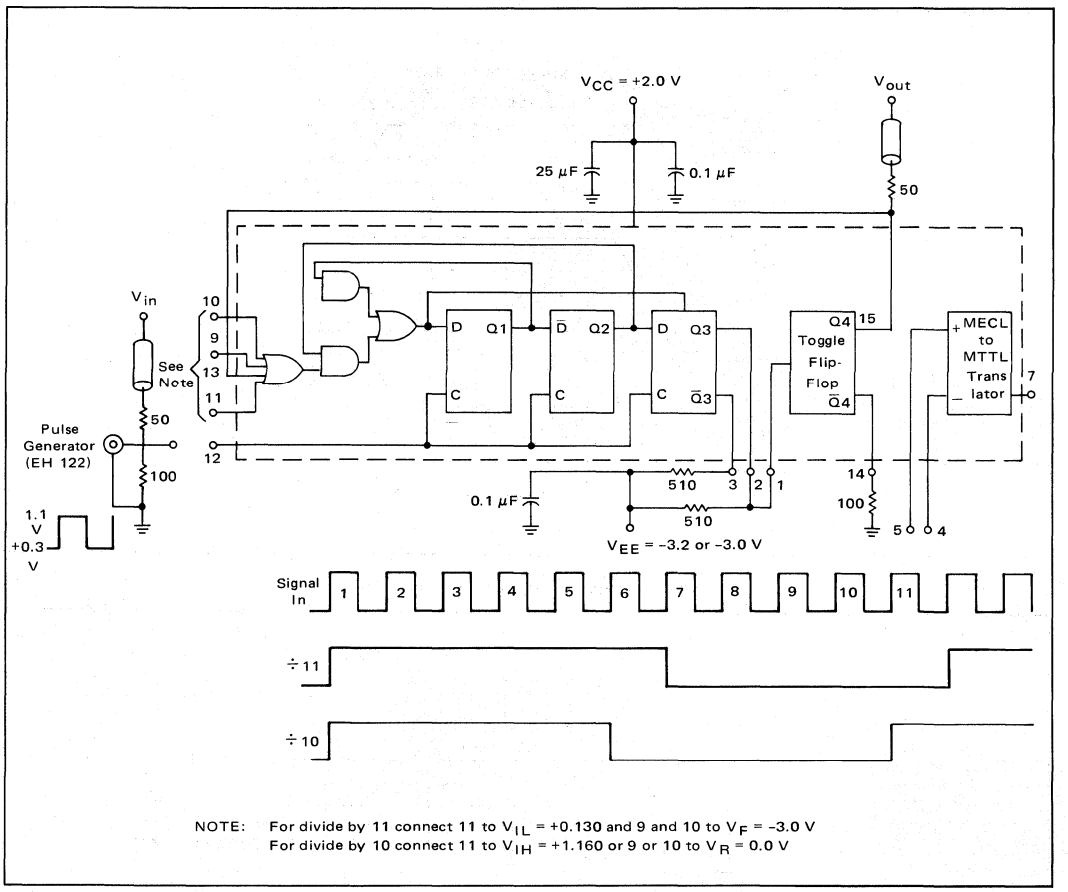


FIGURE 6 – MAXIMUM FREQUENCY TEST CIRCUIT



NOTE: Output Waveforms are same as shown in Figures 4 and 5.

FIGURE 7 – MAXIMUM FREQUENCY TEST CIRCUIT



NOTE: For divide by 11 connect 11 to V_{IL} = +0.130 and 9 and 10 to V_F = -3.0 V
For divide by 10 connect 11 to V_{IH} = +1.160 or 9 or 10 to V_R = 0.0 V

FIGURE 8 – STATE DIAGRAMS

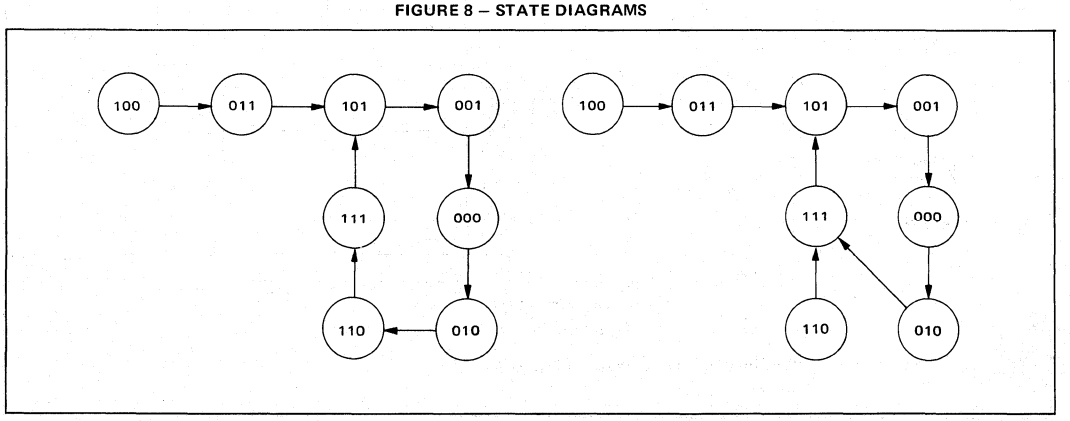
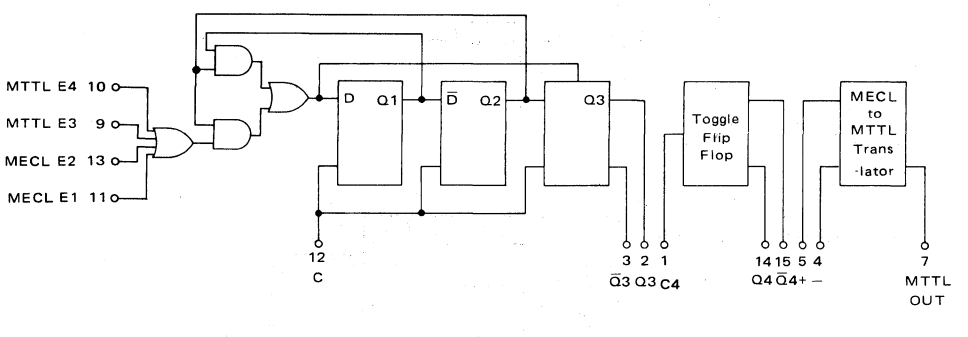


FIGURE 9 – ÷5/6



Divide by 2 use Toggle Flip-Flop

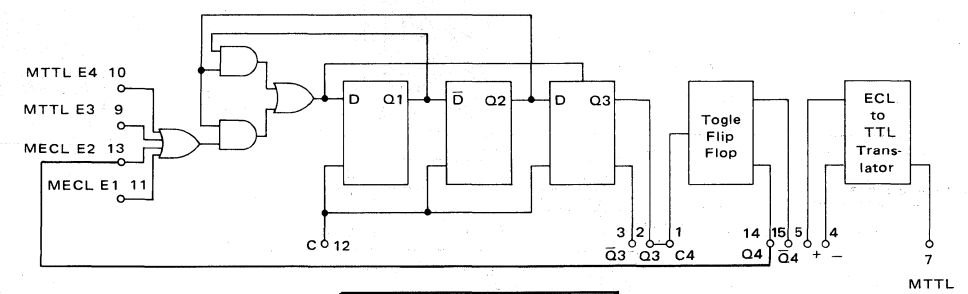
COUNT	Q1	Q2	Q3
6	0	1	1
7	1	1	1
5	1	0	1
1	1	0	0
0	0	0	0
2	0	1	0

E1 + E2 + E3 + E4 = 1

E1 + E2 + E3 + E4 = 0

To obtain a MTTL output connect 5 and 4 to 2 and 3 or 14 and 15 respectively.

FIGURE 10 – ÷10/11



COUNT	Q1	Q2	Q3	Q4
14	0	1	1	1
15	1	1	1	1
13	1	0	1	1
9	1	0	0	1
8	0	0	0	1
10	0	1	0	1
7	1	1	1	0
5	1	0	1	0
1	1	0	0	0
0	0	0	0	0
2	0	1	0	0

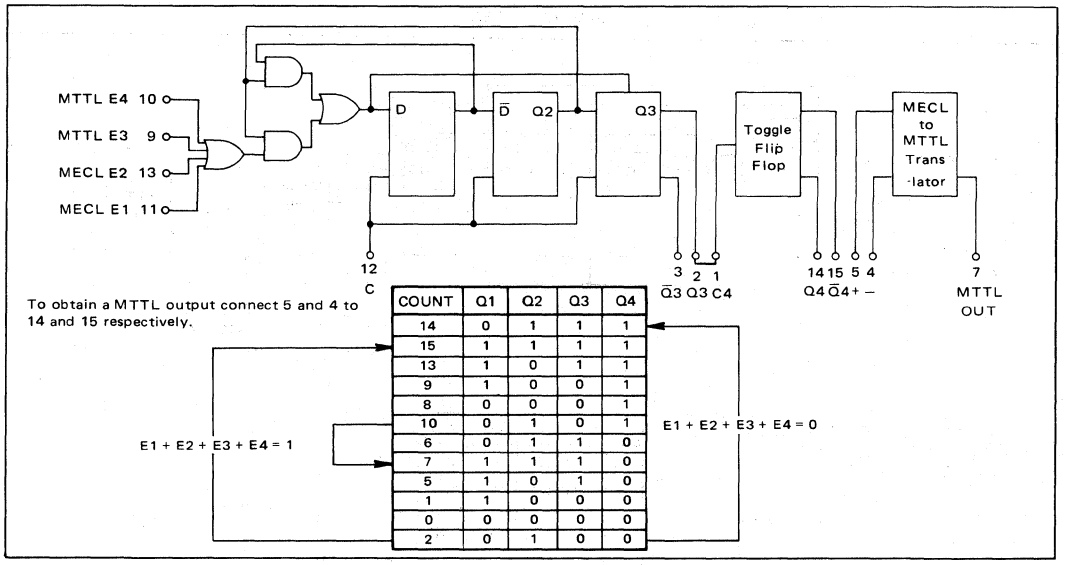
E1 + E3 + E4 = 1

E1 + E3 + E4 = 0

To obtain a MTTL output connect 5 and 4 to 14 and 15 respectively.

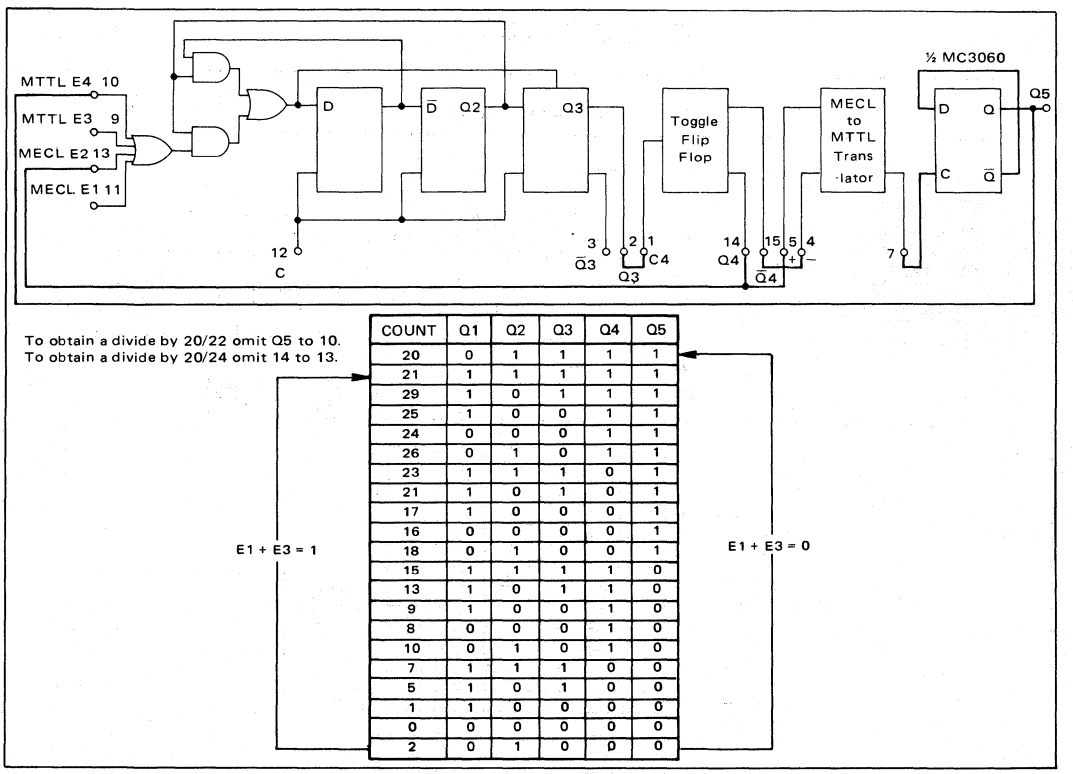
5

FIGURE 11 – - - 10/12



COUNT	Q1	Q2	Q3	Q4
14	0	1	1	1
15	1	1	1	1
13	1	0	1	1
9	1	0	0	1
8	0	0	0	1
10	0	1	0	1
6	0	1	1	0
7	1	1	1	0
5	1	0	1	0
1	1	0	0	0
0	0	0	0	0
2	0	1	0	0

FIGURE 12 - - 20/21



COUNT	Q1	Q2	Q3	Q4	Q5
20	0	1	1	1	1
21	1	1	1	1	1
29	1	0	1	1	1
25	1	0	0	1	1
24	0	0	0	1	1
26	0	1	0	1	1
23	1	1	1	0	1
21	1	0	1	0	1
17	1	0	0	0	1
16	0	0	0	0	1
18	0	1	0	0	1
15	1	1	1	1	0
13	1	0	1	1	0
9	1	0	0	1	0
8	0	0	0	1	0
10	0	1	0	1	0
7	1	1	1	0	0
5	1	0	1	0	0
1	1	0	0	0	0
0	0	0	0	0	0
2	0	1	0	0	0

FUNCTION DESCRIPTION

INTRODUCTION

The MC12012 is one part of a variable modulus (divisor) prescaling subsystem used in certain Digital Phase-Locked Loops (PLL).

More often than not, the feedback loop of any PLL contains a counter-divider. Many methods are available for building a divider, but not all are simple, economical, or convenient in a particular application.

The technique and system described here offer a new approach to the construction of a phase-locked loop divider. In addition to using the MC12012 variable modulus prescaler, this system requires an MC12014 Counter Control Logic function, together with suitable programmable counters (e.g. MC4016s). Data sheets for these additional devices should be consulted for their particular functional descriptions.

THE MC12012 TWO MODULUS PRESCALER

Three functional blocks are contained in the MC12012 variable modulus prescaler: 1) a controllable ÷5/÷6 prescaler; 2) a ÷ 2 prescaler; and 3) an ECL to TTL translator (for single power supply operation).

Selection of division by 5 or by 6 is made by inputs to E1 through E4. If all E inputs are low before the transition of the clock pulse driving Q3 high, Q3 will stay high for 3 clock pulses, then will go low for 3 clock pulses. This provides a divide by 6 function.

On the other hand, if any one or all of the E inputs are high prior to the positive transition of the clock pulse driving Q3 high, Q3 will stay high for only 2 clock pulses, then will go low for 3 clock pulses. The result is division by 5.

For the ÷5 operation, at least one of the E inputs must go high sometime before the clock pulse. This time is referred to as the "setup time." Specifications for setup time are given in the electrical characteristics table: t_{setup1} and t_{setup2} for E1 and E2 (MECL inputs), and E3 and E4 (MTTL inputs).

For the divide by 6 operation all E inputs must be low for some time prior to the clock pulse. This time is referred to as the "release time." Data for release time is given in the electrical characteristics table; t_{re1} and t_{re2} for E1, E2, E3, E4.

The data given in the tables for setup and release times are referenced to the positive transition of the clock pulse causing Q3 to go high. If it is necessary to reference the setup and release times to the positive transition of Q3, add t++ (specified for Q3) to the setup/release times given. It should be noted that the logic states for the enable inputs are important only for only one clock pulse which causes Q3 to go high (within the limits specified by setup and release times).

The ÷ 5/÷ 6 prescaler may be connected externally to the ÷ 2 prescaler to form a ÷ 10/÷ 11 prescaler (Figure 10) or a ÷ 10/÷ 12 prescaler (Figure 11).

By way of an example showing how a ÷ 10/÷ 11 prescaler operates, note that if E1, E3, and E4 (Figure 10) are held in a low state, the counter divides by 11. To do this, a feedback connection is established from Q4 to E2 (or to E1). With this feedback, the ÷ 5/÷ 6 prescaler divides by 5 when Q4 is high, and by 6 when Q4 is low.

Since Q4 changes state with each positive transition of Q3, the prescaler alternates between ÷ 5 and ÷ 6 resulting in a ÷ 11 at Q4.

If any one or all of the E inputs are high (Figure 10), the 5/6 prescaler always divides by 5 and a divide by 10 results at Q4.

With the addition of external flip-flops and counters (MECL or MTTL) various other modulus prescalers may be produced (20/21, 20/22, 20/24, 40/41, 50/51, 100/101, etc.).

THE TECHNIQUE OF DIRECT PROGRAMMING BY UTILIZING A TWO MODULUS PRESCALER (MC12012)

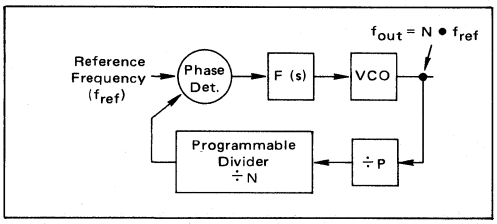
The disadvantage of using a fixed modulus (÷ P) for frequency division in high frequency phase-locked loops (PLL) is that it requires dividing the desired reference frequency by P also (desired reference frequency equals channel spacing.)

The MC12012 is specially designed for use with a technique called "variable modulus prescaling". This technique allows a simple MECL two-modulus prescaler (MC12012) to be controlled by a relatively slow MTTL programmable counter. The use of this technique permits direct high-frequency prescaling without any sacrifice in resolution since it is no longer necessary to divide the reference frequency by the modulus of the high frequency prescaler.

The theory of "variable modulus prescaling" may be explained by considering the system shown in Figure 13. For the loop shown:

$$f_{out} = N \bullet P \bullet f_{ref} \quad (1)$$

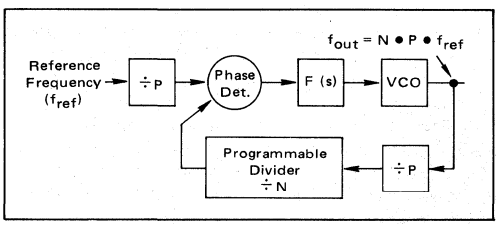
FIGURE 13 – FREQUENCY SYNTHESIS BY PRESCALING



where P is fixed and N is variable. For a change of 1 in N, the output frequency changes by $P \bullet f_{ref}$. If f_{ref} equals the desired channel spacing, then only every P channel may be programmed using this method. A problem remains: how to program intermediate channels.

One solution to this problem is shown in Figure 14.

FIGURE 14 – FREQUENCY SYNTHESIS BY PRESCALING



A ÷ P is placed in series with the desired channel spacing to give a reference frequency: channel spacing/P.

Another solution is found by considering the defining equation (1) for f_{out} of Figure 13. From the equation it may be seen that only every P channel can be programmed simply, because N is always an integer. To obtain intermediate channels, P must be multiplied by an integer plus a fraction. This fraction would be of the form: A/P. If N is defined to be an integer number, Np, plus a fraction, A/P, N may be expressed as:

$$N = Np + A/P.$$

Substituting this expression for N in equation 1 gives:

$$f_{out} = (Np + A/P) \bullet P \bullet f_{ref} \quad (2)$$

or:

$$f_{out} = (Np\ P + A) \bullet f_{ref} \quad (3)$$

$$f_{out} = Np \bullet P \bullet f_{ref} + A \bullet f_{ref}. \quad (4)$$

Equation 4 shows that all channels can be obtained directly if N can take on fractional values. Since it is difficult to multiply by a fractional number, equation 4 must be synthesized by some other means.

Taking equation 3 and adding ±AP to the coefficient of f_{ref}, the equation becomes:

$$f_{out} = (Np \bullet P + A + A \bullet P - A \bullet P)\ f_{ref}. \quad (5)$$

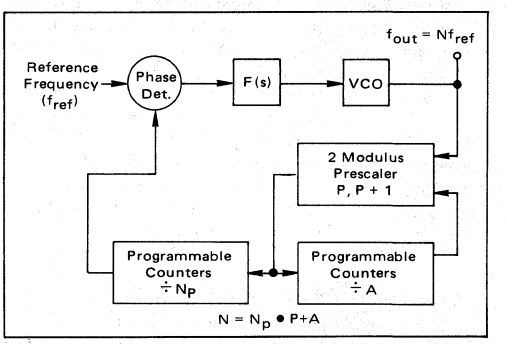
Collecting terms and factoring gives:

$$f_{out} = [(Np - A)\ P + A\ (P + 1)]\ f_{ref} \quad (6)$$

From equation 6 it becomes apparent that the fractional part of N can be synthesized by using a two-modulus counter (P and P + 1) and dividing by the upper modulus, A times, and the lower modulus (Np - A) times.

This equation (6) suggests the circuit configuration in Figure 15. The A counter shown must be the type that

FIGURE 15 – FREQUENCY SYNTHESIS BY TWO MODULUS PRESCALING



counts from the programmed state (A) to the enable state, and remains in this state until divide by Np is completed in the programmable counter.

In operation, the prescaler divides by P + 1, A times. For every P + 1 pulse into the prescaler, both the A counter and Np counter are decremented by 1. The prescaler divides by P + 1 until the A counter reaches the zero state. At the end of (P + 1) • A pulses, the state of the Np counter equals (Np - A). The modulus of the prescaler then changes to P. The variable modulus counter divides by P until the remaining count, (Np - A) in the Np counter, is decremented to zero. Finally, when this is completed, the A and Np counters are reset and the cycle repeats.

To further understand this prescaling technique, consider the case with P = 10. Equation 6 becomes:

$$f_{out} = (A + 10\ Np) \bullet f_{ref} \quad (7)$$

If Np consists of 2 decades of counters then:

$$Np = 10\ N_0 + N_1$$

(N_0 is the most significant digit),

and equation 7 becomes:

FIGURE 16 – DIRECT PROGRAMMING UTILIZING TWO-MODULUS PRESCALER

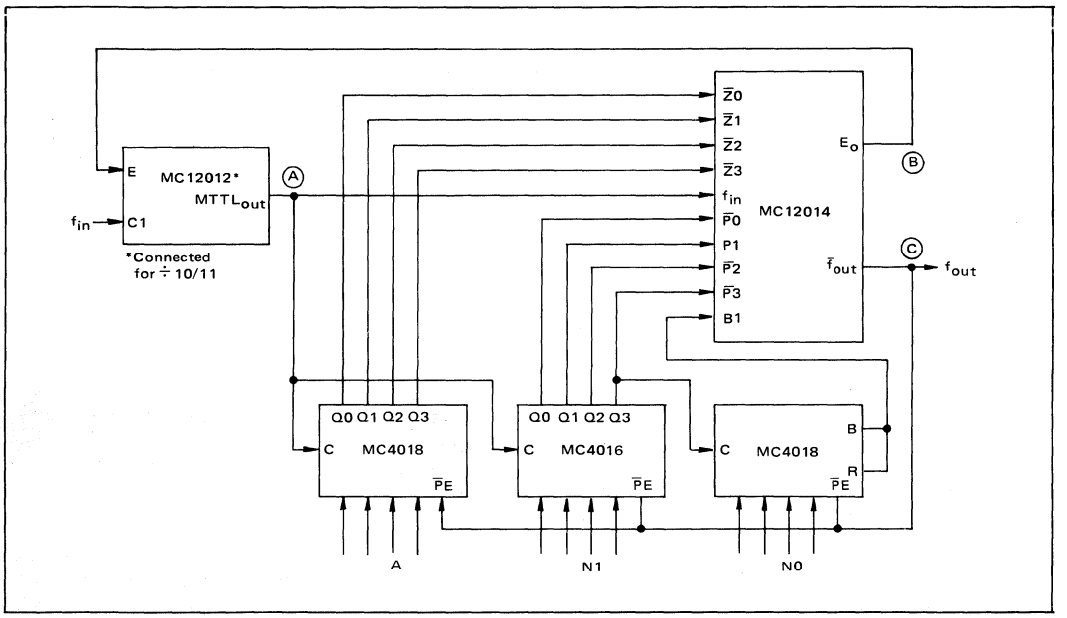


FIGURE 17 – WAVEFORMS FOR DIVIDE BY 43

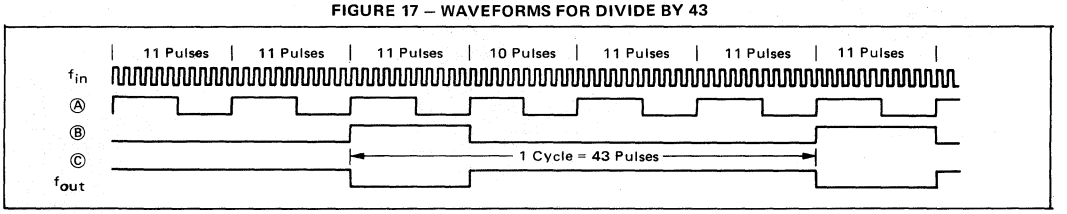


FIGURE 18 – WAVEFORMS FOR DIVIDE BY 42

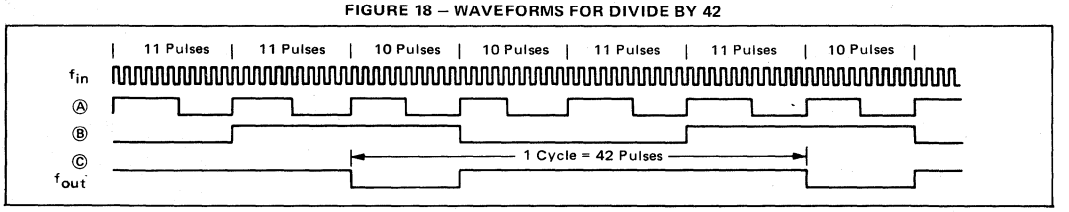
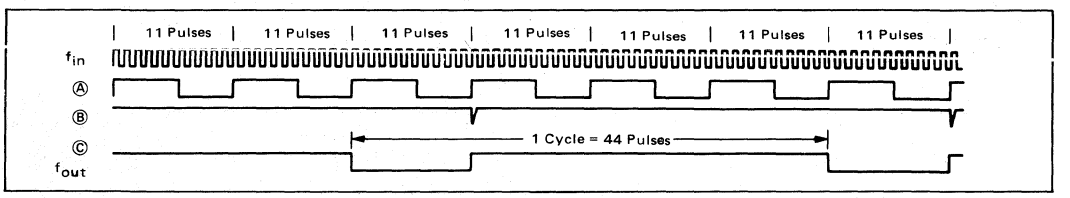


FIGURE 19 – WAVEFORMS FOR DIVIDE BY 44



$$f_{out} = (100\,N_0 + 10\,N_1 + A)\,f_{ref}.$$

To do variable modulus prescaling using the MC12012 and programmable divide by N counters (MC4016, MC-4018), one additional part is required: the MC12014 (Counter Control Logic).

In variable modulus prescaling the MC12014 serves a dual purpose: it detects the terminal (zero) count of the A counter, to switch the modulus of the MC12012; and it extends the maximum operating frequency of the programmable counters to above 25 MHz. (See the MC12014 data sheet for a detailed description of the Counter Control Logic).

Figure 16 shows the method of interconnecting the MC12012, MC12014, and MC4016 (or MC4018) for variable modulus prescaling. To understand the operation of the circuit shown in Figure 16, consider division by 43. Division by 43 is done by programming $N_0 = 0$, $N_1 = 4$, and $A = 3$.

Waveforms for various points in the circuit are shown in Figure 17 for this division. From the waveforms it may be seen that the two-modulus prescaler starts in the divide by 11 mode, and the first input pulse causes point A to go high. This positive transition decrements the upper counter (Np) to 3, and the lower counter (A) to 2.

After 11 pulses, point A again goes high; the upper counter decrements to 2 and the lower counter to 1. The "2" contained in the upper counter enables the inputs to the frequency extender portion of the MC12014. After 11 more pulses point A goes high again.

With this position transition at A, the output (f_{out}) of the MC12014 goes low, the upper counter goes to 1, and the lower counter goes to 0. The zero state of the lower counter is detected by the MC12014, causing point B to go to 1 and changing the modulus of the MC12012 to 10 at the start of the cycle.

When f_{out} goes low, the programmable counters are reset to the programmed number. After 11 pulses (the enable went high after the start of the cycle and therefore doesn't change the modulus until the next cycle), point A makes another positive transition. This positive transition causes f_{out} to return high, release the preset on the counter, and generates a pulse to clear the latch (return point B to 0).

After 10 pulses the cycle begins again (point B was high prior to point A going high). The number of input pulses that have occured during this entire operation is: 11 + 11 + 11 + 10 = 43. Figures 18 and 19 show the waveforms for divide by 42 and divide by 44 respectively.

The variable modulus prescaling technique may be used in any application as long as the number in the Np counter is greater than or equal to the number in the A counter. Failure to observe this rule will result in erroneous results. (For example, for the system shown in Figure 16 if the number 45 is programmed, the circuit actually will divide by 44. This is not a serious restriction since Np is greater than A in most applications).

It is important to note that the A counter has been composed of only one counter for discussion only; where required, the A counter may be made as large as needed by cascading several programmable counters. Figure 20 shows the method of interconnecting counters. Operation is previously described. The number of stages in the A counter should not exceed the number of stages for the

5

FIGURE 20 – METHOD OF INTERCONNECTING COUNTERS

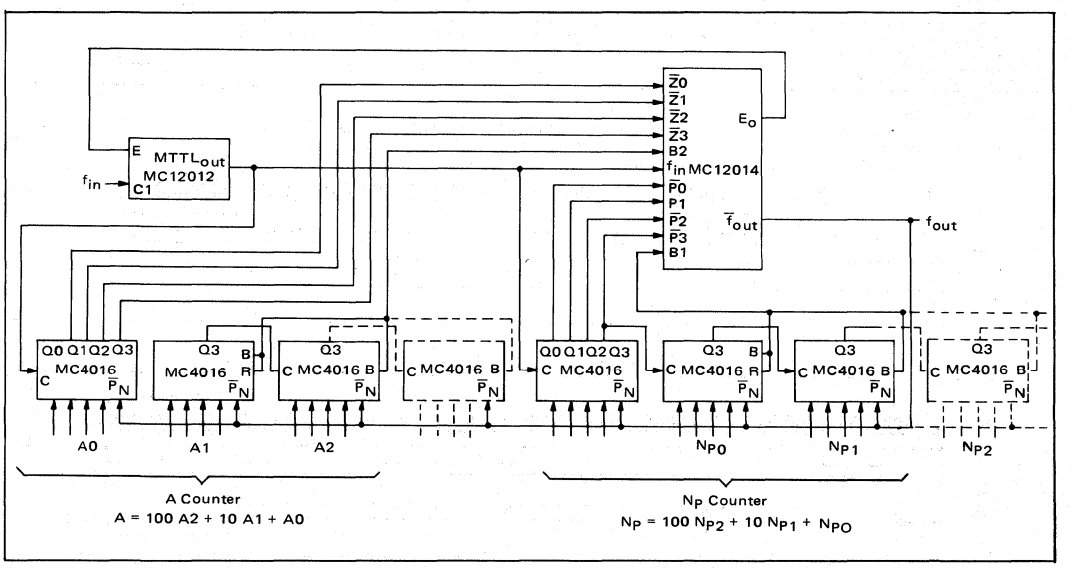


FIGURE 21 – DIRECT PROGRAMMING 100-200 MHz SYNTHESIZER IN 50 kHz STEPS

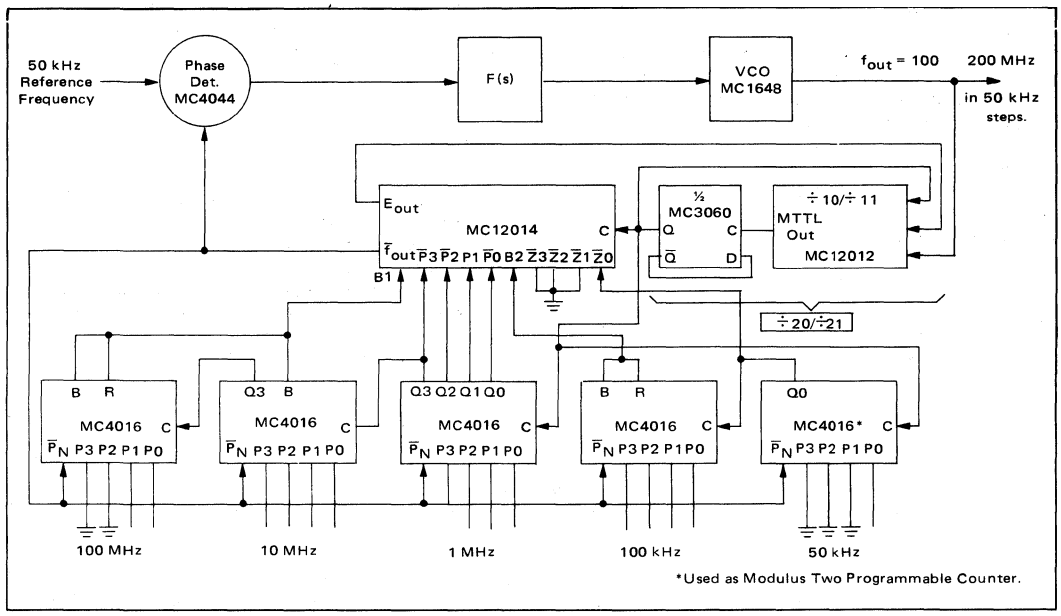
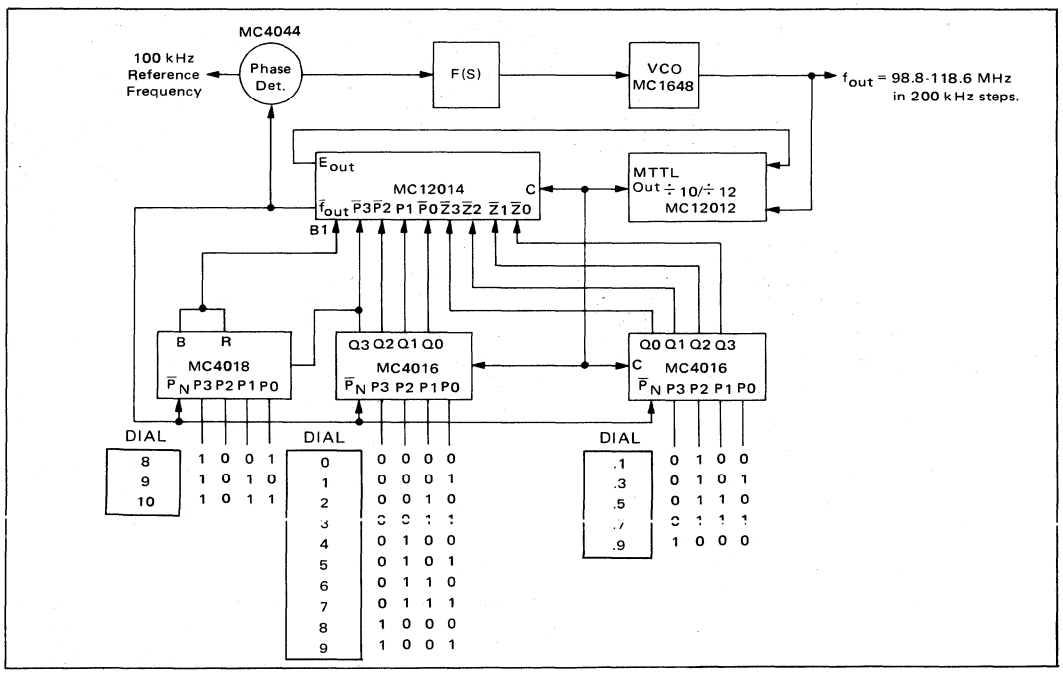


FIGURE 22 – FM BAND SYNTHESIZER WITH 10.7 MHz I.F. OFFSET



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Np counters. As many counters as desired may be cascaded, as long as fan-in and fan-out rules for each part are observed.

The theory of "variable modulus prescaling" developed above, examined a case in which the upper modulus of the two-modulus prescaler was 1 greater than the lower modulus. However, the technique described is by no means limited to this one special case. There are applications in which it is desirable to use moduli other than P/(P + 1).

It can be shown that for a general case in which the moduli of the two-modulus prescaler are P and P + M, equation 6 becomes:

$$f_{out} = [(Np - A)\,P + A\,(P + M)] \bullet f_{ref}$$

or

$$f_{out} = [Np \bullet P + M \bullet A] \bullet f_{ref}. \qquad (8)$$

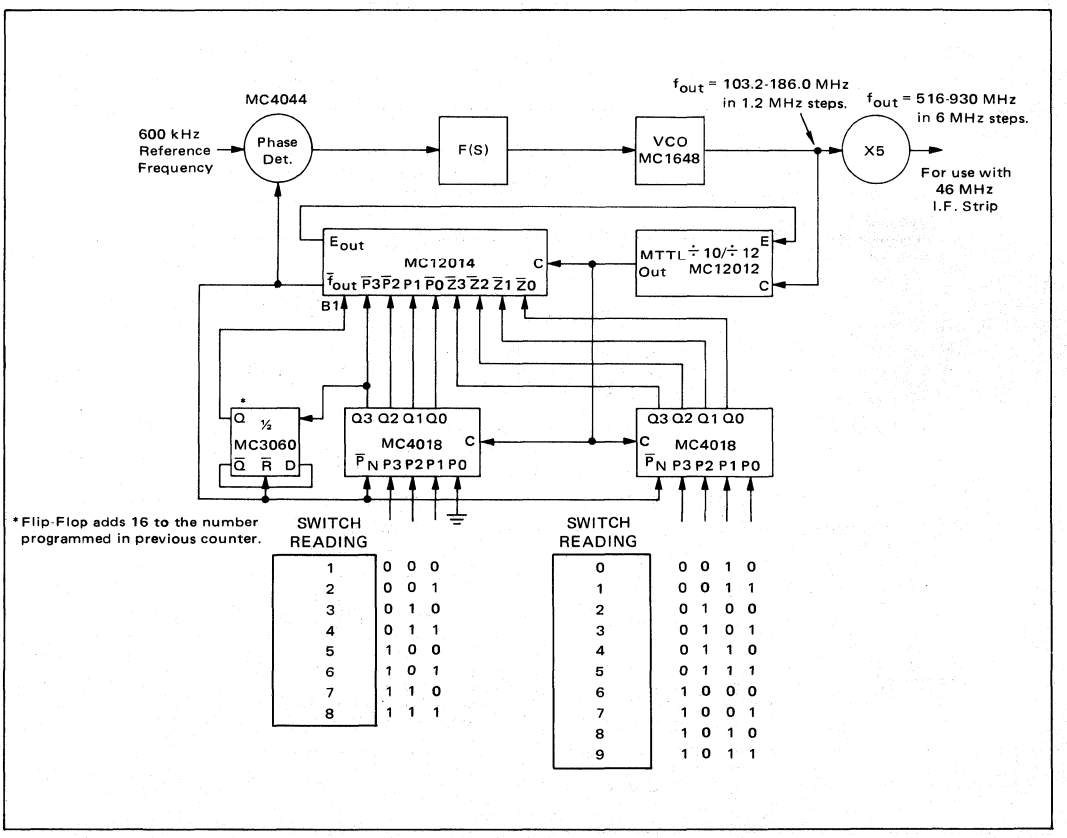
From equation 8 it may be seen that the upper modulus of the two-modulus prescaler has no effect on the Np counter, and that the number programmed in the A counter is simply multiplied by M.

APPLICATIONS

There is no one procedure which will always yield the best counter configuration for all possible MC12012 applications. Each designer will develop his own special design for the counter portion of his PLL system.

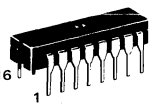
An insight into some of the various possible counter schemes may be obtained by considering the various PLL systems shown in Figures 21, 22, and 23. These examples were chosen to show some of the moduli that may be obtained by using the MC12012.

FIGURE 23 – UHF SYNTHESIZER USING 10/12 COUNTER

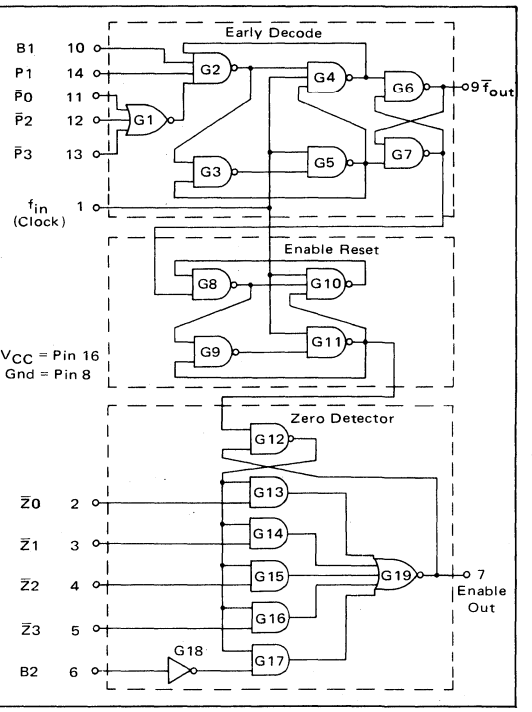


MC12014

The MC12014 monolithic counter control logic unit is designed for use with the MC12012 Two-Modulus Prescaler and the MC74416 Programmable Counter to accomplish direct high-frequency programming. The MC12014 consists of a zero detector which controls the modulus of the MC12012, and an early decode function which controls the MC74416. The early decode feature also increases the useful frequency range of the MC74416 from 8.0 MHz to 25 MHz.



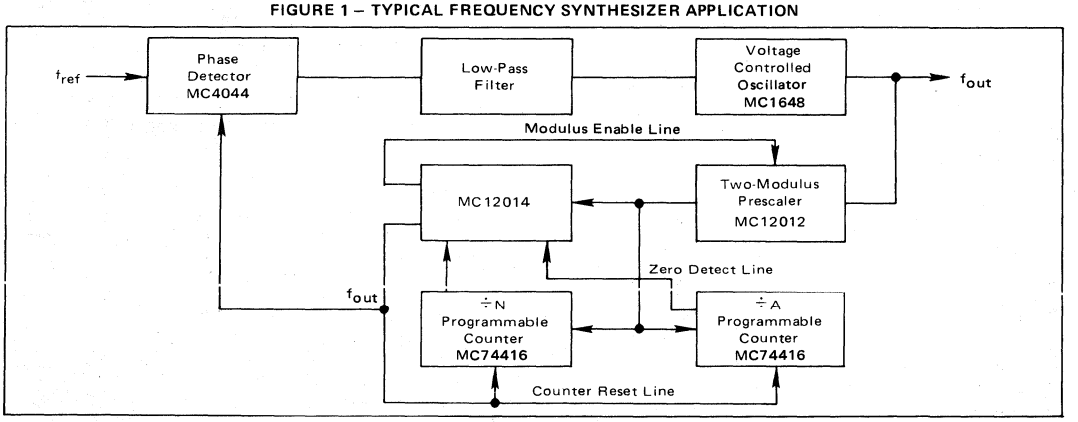
CERAMIC PACKAGE
CASE 620



MAXIMUM RATINGS

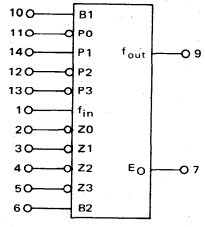
Rating	Symbol	Unit
Supply Operating Voltage Range	4.75 to 5.25	Vdc
Supply Voltage	+7.0	Vdc
Input Voltage	+5.5	Vdc
Output Voltage	+5.5	Vdc
Operating Temperature Range	0 to +75	°C
Storage Temperature Range	-65 to +150	°C
Maximum Junction Temperature	+150	°C
Thermal Resistance – Junction to Case (θ_{JC})	0.05	°C/mW
Thermal Resistance – Junction to Ambient (θ_{JA})	0.15	°C/mW

FIGURE 1 – TYPICAL FREQUENCY SYNTHESIZER APPLICATION



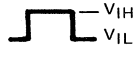
ELECTRICAL CHARACTERISTICS

Test procedures are shown for the f_{in}, $\overline{Z0}$, B1 and P1 inputs. All other inputs are tested in the same manner as the $\overline{Z0}$ input.



Characteristic	Symbol	Pin Under Test	Test Limits 0 to +75°C Min	Max	Unit	TEST CURRENT/VOLTAGE VALUES (All Temperatures) mA I_{OL}	I_{OH}	I_{IC}	Volts V_{IL}	V_{IH}	V_{IHH}	V_{RH}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
						16	-1.6	-10	0.5	2.4	5.5	4.5	5.0	4.75	5.25	
						TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW.										
Input																
Forward Current	I_{IL}	1	–	-6.4	mAdc	–	–	–	1	–	–	–	–	–	16	8,10
		2	–	-1.6	↓	–	–	–	2	–	–	–	–	–	↓	8
		10	–	↓	↓	–	–	–	10	–	–	–	–	–	↓	1,8,11,12,13
		14	–	↓	↓	–	–	–	14	–	–	–	–	–	↓	1,8,11,12,13
Leakage Current	I_{IH}	1	–	160	μAdc	–	–	–	–	1	–	–	–	–	16	8,10
		2	–	40	↓	–	–	–	–	2	–	–	–	–	↓	8
		10	–	↓	↓	–	–	–	–	10	–	–	–	–	↓	1,8,11,12,13
		14	–	↓	↓	–	–	–	–	14	–	–	–	–	↓	1,8,11,12,13
	I_{IHH}	1	–	1.0	mAdc	–	–	–	–	–	1	–	–	–	16	8
		2	–	↓	↓	–	–	–	–	–	2	–	–	–	↓	8
		10	–	↓	↓	–	–	–	–	–	10	–	–	–	↓	1,8,11,12,13
		14	–	↓	↓	–	–	–	–	–	14	–	–	–	↓	1,8,11,12,13
Clamp Voltage	V_{IC}	1	–	-1.2	Vdc	–	–	1	–	–	–	–	–	16	–	8
		2	–	↓	↓	–	–	2	–	–	–	–	–	↓	–	↓
		10	–	↓	↓	–	–	10	–	–	–	–	–	↓	–	
		14	–	↓	↓	–	–	14	–	–	–	–	–	↓	–	
Output																
Output Voltage	V_{OL}*	7	–	0.5	Vdc	7	–	–	11,12,13	–	–	2,3,4,5,10,11	–	16	–	8
		9	–	0.5	Vdc	9	–	–	11,12,13	–	–	10,14	–	16	–	8
	V_{OH}	7	2.4	–	Vdc	–	7	–	2,3,4,5	–	–	6	–	16	–	8
		9**	2.4	–	Vdc	–	9	–	–	–	–	11,12,13	–	16	–	8
Short-Circuit Current	I_{OS}	7	-20	-65	Vdc	–	–	–	2,3,4,5	–	–	6	16	–	–	7,8
		9**	-20	-65	Vdc	–	–	–	–	–	–	11,12,13	16	–	–	8,9
Power Requirements																
Power Supply Drain	I_{CC}	16	–	35	mAdc	–	–	–	–	–	–	–	16	–	–	1,8

*Output level to be measured after waveform 1 is applied to f_{in}, pin 1.
**Output level to be measured after waveform 2 is applied to f_{in}, pin 1.

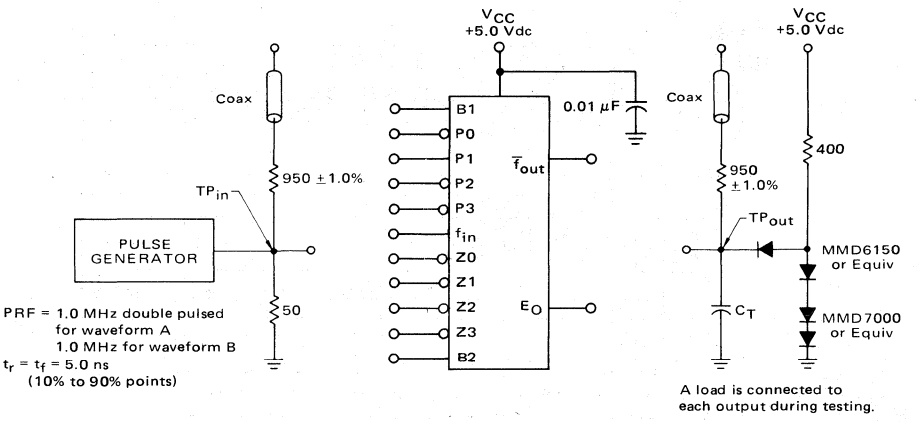
Waveform 1: 

Waveform 2: 

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, waveform letters refer to waveforms on next page.)

Characteristic	Symbol	Pin Under Test		Test Limits (ns)							Pulse Gen. 1		Pulse Gen. 2		Pulse Out		Voltage Applied to Pins Listed Below	
				0°C		+25°C			+75°C									
		In	Out	Min	Max	Min	Typ	Max	Min	Max	Wave-form	Pin	Wave-form	Pin	Wave-form	Pin	V_{IL} = 0.5 V	V_{IH} = 2.4 V
Propagation Delay	t_{PLH1}	1	9	7.0	15	7.0	10	15	7.0	17	A	1	J	10	K	9	11,12,13	14
	t_{PHL1}	1	9	7.0	16	7.0	11	16	7.0	18	A	1	J	10	K	9	11,12,13	14
	t_{PLH2}	2	7	5.0	12	5.0	8.5	12	5.0	14	A	1	H	2	L	7	3,4,5,11,12,13	6,10,14
		3	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	3	↓	↓	2,4,5,11,12,13	↓
		4												4			2,3,5,11,12,13	
		5												5			2,3,4,11,12,13	
	t_{PHL2}	1	7	7.0	16	7.0	11	16	7.0	18	A	1	H	2	L	7	3,4,5,11,12,13	6,10,14
	t_{PLH3}	6	7	7.0	16	7.0	11	16	7.0	18	A	1	J	6	L	7	2,3,4,5,11,12,13	10,14
Setup Time	$t_{setup"1"}$	10	–	–	–	–	1.0	2.0	–	–	A	1	B	10	G	9	11,12,13	14
		11	–	–	–	–	7.0	12	–	–	↓	↓	↓	11	F	↓	12,13	10,14
		12	–	–	–	–	↓	↓	–	–				12			11,13	↓
		13	–	–	–	–			–	–				13	↓		11,12	
		14	–	–	–	–	1.0	2.0	–	–				14	G		11,12,13	10
	$t_{setup"0"}$	10	–	–	–	–	4.5	8.0	–	–	A	1	C	10	F	9	11,12,13	14
		11	–	–	–	–	5.0	9.0	–	–	↓	↓	↓	11	G	↓	12,13	10,14
		12	–	–	–	–	↓	↓	–	–				12			11,13	↓
		13	–	–	–	–			–	–				13	↓		11,12	
		14	–	–	–	–	4.5	8.0	–	–				14	F		11,12,13	10
Hold Time	$t_{hold"1"}$	10	–	–	–	–	4.0	8.0	–	–	A	1	D	10	G	9	11,12,13	14
		11	–	–	–	–	5.0	10	–	–	↓	↓	↓	11	F	↓	12,13	10,14
		12	–	–	–	–	↓	↓	–	–				12			11,13	↓
		13	–	–	–	–			–	–				13	↓		11,12	
		14	–	–	–	–	4.0	8.0	–	–				14	G		11,12,13	10
	$t_{hold"0"}$	10	–	–	–	–	1.0	2.0	–	–	A	1	E	10	F	9	11,12,13	14
		11	–	–	–	–	7.5	14	–	–	↓	↓	↓	11	G	↓	12,13	10,14
		12	–	–	–	–	↓	↓	–	–				12			11,13	↓
		13	–	–	–	–			–	–				13	↓		11,12	
		14	–	–	–	–	1.0	2.0	–	–				14	F		11,12,13	10

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

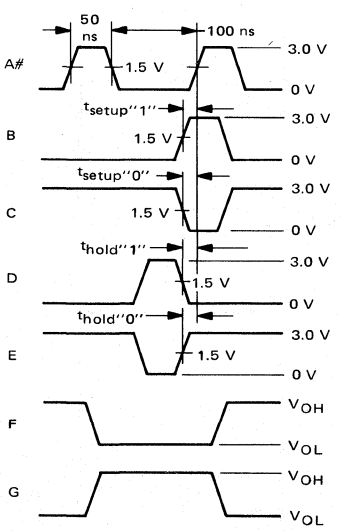


Two pulse generators are required and must be slaved together to provide the waveforms shown.

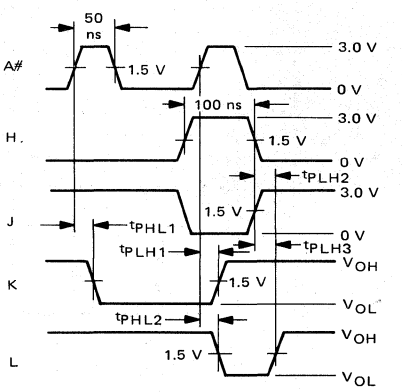
C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

SETUP AND HOLD TIMES



PROPAGATION DELAY TIMES

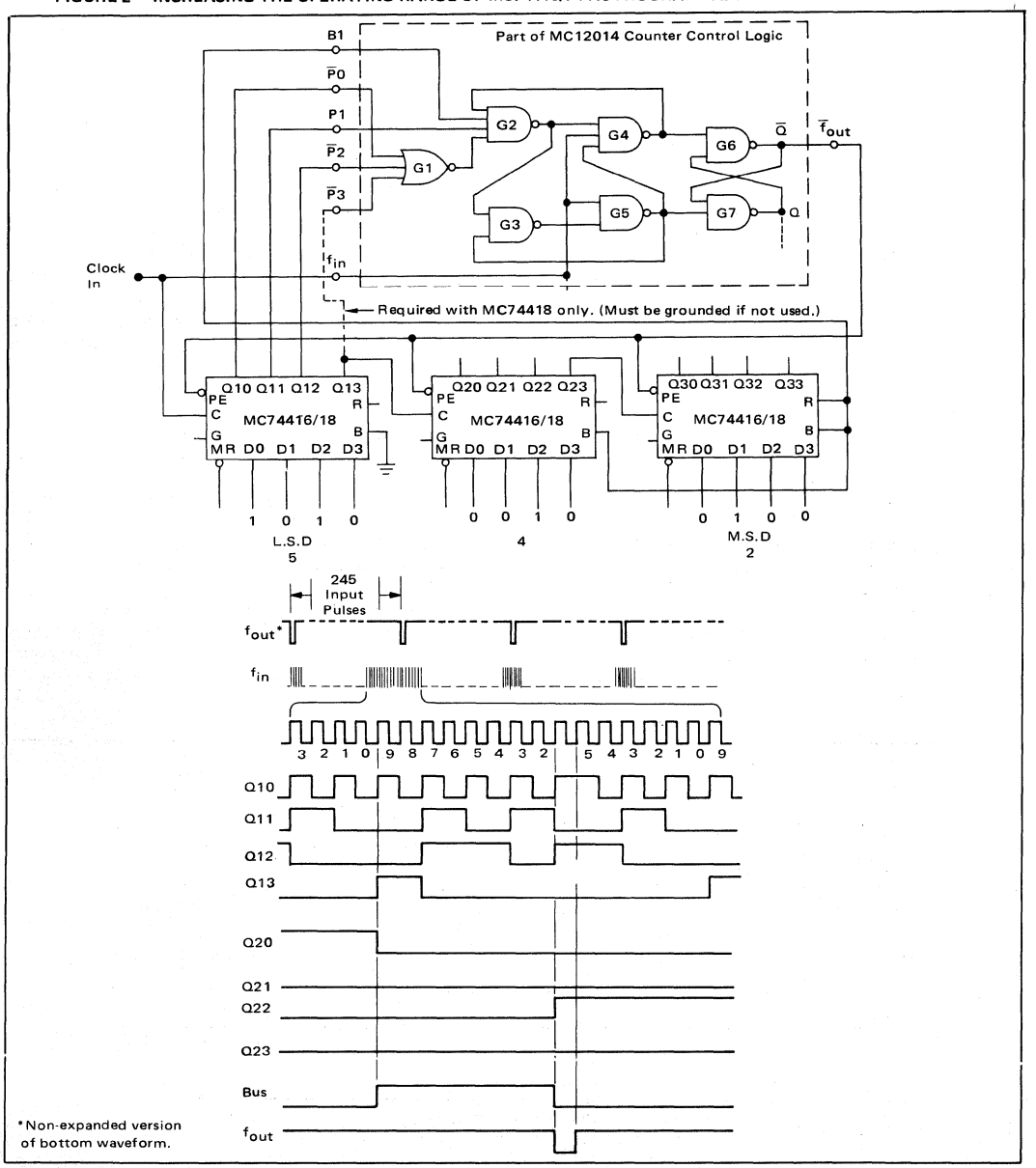


#Pulse A (f_{in}) used with all tests.

APPLICATIONS INFORMATION

The MC12014 Counter Control Logic incorporates two features for enhancing operation of the MC74416/74418 Programmable Counters.[1] Maximum operating frequency of the counters is limited by the time required for re-programming at the end of each count-down cycle. Operation can be extended to approximately 25 MHz by using the "early decode" feature included in the MC12014 The appropriate connections are shown in Figure 2. Only

FIGURE 2 – INCREASING THE OPERATING RANGE OF MC74416/74418 PROGRAMMABLE COUNTERS USING MC12014



1 See the MC54416/54418 data sheet for additional information.

three counter stages are shown; however, up to eight stages can be satisfactorily cascaded. Note the following differences between this and the non-extended method: the counter gate inputs are not connected to the input clock; all parallel enables are connected to the $\overline{Q}$ output (f_{out}) of a type D flip-flop formed by gates G2 through G7 in the MC12014 package; the bus terminal of the least significant stage is grounded; all other bus terminals and one internal resistor, R, are connected together and serve as a data input, B1, to the flip-flop. Four additional data inputs, $\overline{P0}$ through $\overline{P3}$, serve to decode the "two" state of the least significant counter stage. Circuit operation is illustrated in waveforms of Figure 2, where the timing for the end of a count-down cycle is shown in expanded form. The counter parallel inputs are assumed to have N = 245 programmed. Timing is not shown for the third stage since it has already been counted down to the all zero state. As the next-to-least significant stage reaches zero, the common bus line goes high. Count down of the least significant stage continues until the "two" state is reached, causing the remaining data inputs to the flip-flop to go high. The next-to-last clock pulse of the cycle then triggers the flip-flop $\overline{Q}$ output low. This takes the parallel enables of all three counter stages low, resetting the programmed data to the outputs. The next input pulse clocks $\overline{Q}$ back to the high state since the data inputs to the flip-flop are no longer all high. The resulting negative output pulse at f_{out} is one input clock period in duration. Note that division by N equal to 001 or 002 is not available using this method.

The frequency synthesizer shown in Figure 8 requires that the programmable counters be quickly stopped after reaching their terminal (zero) count. This can be simply accomplished by taking the master reset of all stages low at the appropriate time. The bus output of the counters could be used for this function since a transition there signals the end of a count-down sequence. However, due to the relatively long delay between the last positive clock transition and the bus transition a faster method is required in this application.

The "zero detection" feature of the MC12014 provides a convenient means of implementing a faster method. Gates G12 through G19 form a latch whose output goes high if B2 is high and low logic levels are applied to the Z0 thru Z3 inputs. When once set to a one by appropriate input conditions, the output of G19 remains high until it is reset by the circuit comprised of gates G8 through G11. Note that since the required information is stored, the counter can be allowed to continue cycling.

The G8-G11 circuit monitors the G7 output of the "early decode" type D flip-flop. When the counter stage connected to the $\overline{P0}$ thru $\overline{P3}$ inputs has counted down to its two state the output of G7 goes high; this enables the G8-G11 circuitry and the next positive clock transition causes the output of G11 to go high, resetting the output of G19 to zero.

Operation of the Counter Control Logic can be further clarified by considering a typical system application for programmable counters illustrated in the frequency synthesizer shown in Figure 3. There the counter provides a means of digitally selecting some integral multiple of a stable reference frequency. The circuit phase locks the output, f_{VCO}, of a voltage controlled oscillator to a reference frequency, f_{ref}.[2] Circuit operation is such that $f_{VCO} = Nf_{ref}$, where N is the divider ratio of the feedback counter, permitting frequency selection by means of thumbwheel switches.

In many synthesizer applications the VCO is operated at VHF frequencies too high for direct division by TTL counters. In these cases the VCO output is usually prescaled by using a suitable fixed divide-by-M ECL circuit as shown in Figure 4. For this configuration, $f_{VCO} = NMf_{ref}$, where N is variable (programmable) and M is fixed. Design of the optimum loop filter requires that the input reference frequency be as high as possible where the upper limit is established by the required channel

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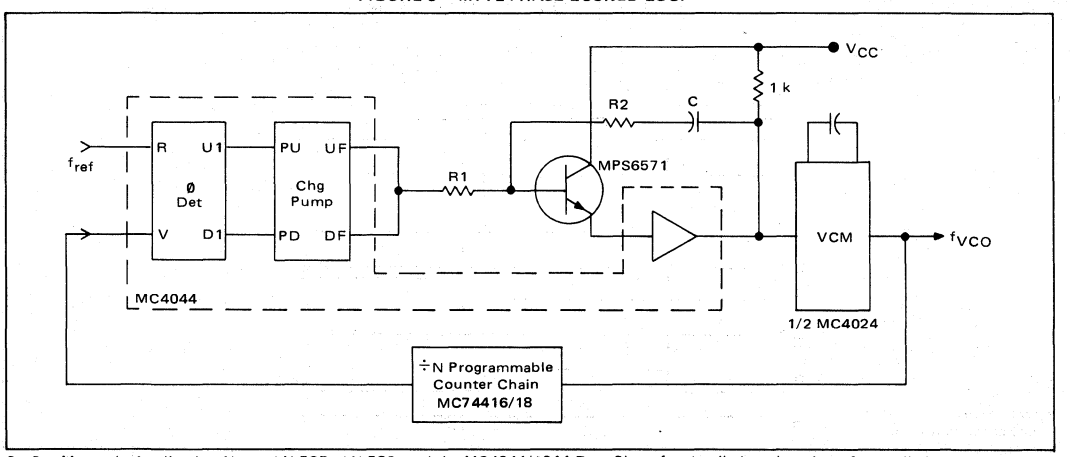
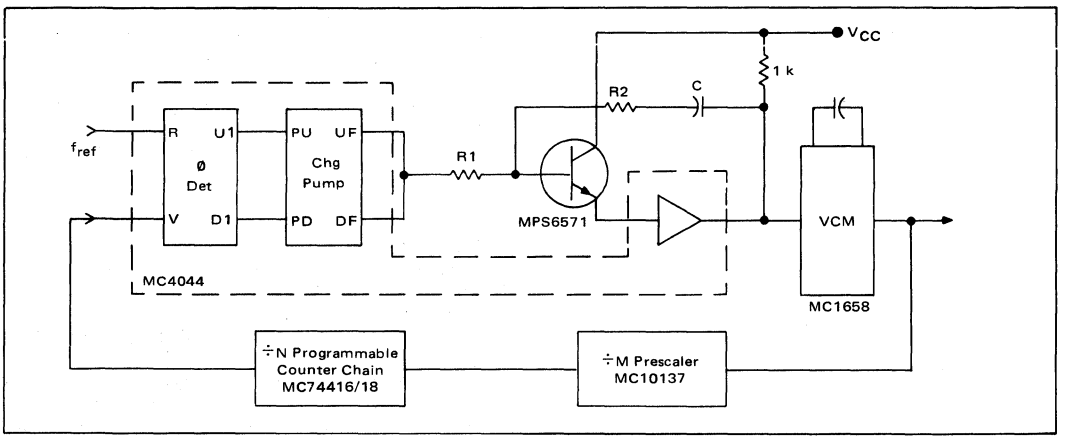
FIGURE 3 – MTTL PHASE-LOCKED LOOP



2 See Motorola Application Notes AN-535, AN-532, and the MC4344/4044 Data Sheet for detailed explanation of over-all circuit operation.

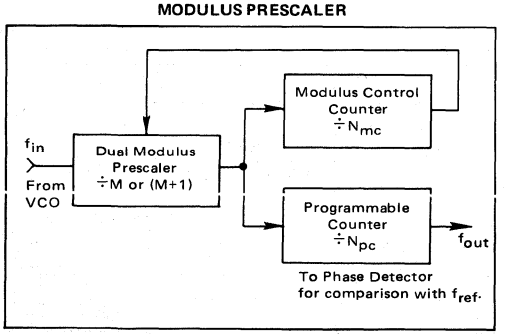
FIGURE 4 – MTTL-MECL PHASE-LOCKED LOOP



spacing. Since $f_{VCO} = Nf_{ref}$ in the non-prescaled case, if N is changed by one, the VCO output changes by f_{ref}, or the synthesizer channel spacing is just equal to f_{ref}. When the prescaler is used as in Figure 4, $f_{VCO} = NMf_{ref}$, and a change of one in N results in the VCO changing by Mf_{ref}, i.e., if f_{ref} is set equal to the minimum permissible channel spacing as is desirable, then only every M channels in a given band can be selected. One solution is to set f_{ref} = channel spacing/M but this leads to more stringent loop filter requirements.

An alternate approach that avoids this problem is provided by the counter configuration shown in Figure 5. It too uses a prescaler ahead of a programmable counter, however the modulus of the prescaler is now controlled by a third counter, causing it to alternate between M and M + 1. Operation is best explained by assuming that all three counters have been set for the beginning of a cycle: the prescaler for division by (M + 1), the modulus control counter for division by N_{mc}, and the programmable counter for division by N_{pc}. The prescaler will divide by (M +1) until the modulus control counter has counted down to zero; at this time, the all zero state is detected and causes the prescaler to divide by M until the programmable counter has also counted down to zero. When this occurs, a cycle is complete and each counter is reset to its original modulus in readiness for the next cycle.

FIGURE 5 – FEEDBACK COUNTERS WITH DUAL MODULUS PRESCALER



To determine the relationship between f_{out} and f_{in}, let T_1 be the time required for the modulus control counter to reach its terminal count and let T_2 be the remainder of one cycle. That is, T_2 is the time between terminal count in the modulus control counter and terminal count in the programmable counter. When the modulus control counter reaches zero, N_{mc} pulses will have entered it at a rate given by $f_{in}/(M + 1)$ pulses/second or T_1 is:

$$T_1 = \frac{(M + 1)}{f_{in}} \bullet N_{mc} \qquad (1)$$

At this time, N_{mc} pulses have also entered the programmable counter and it will reach its terminal counter after $(N_{pc} - N_{mc})$ more pulses have entered. The rate of entry is now f_{in}/M pulses/second since the prescaler is now dividing by M. From this T_2 is given by:

$$T_2 = \frac{M}{f_{in}} \bullet (N_{pc} - N_{mc}) \qquad (2)$$

Since $f = \frac{1}{T}$:

$$f_{out} = \frac{1}{T_{total}} = \frac{1}{T_1 + T_2} = \frac{1}{\frac{(M + 1)N_{mc}}{f_{in}} + \frac{M(N_{pc} - N_{mc})}{f_{in}}} \qquad (3)$$

$$f_{out} = \frac{f_{in}}{(M+1)N_{mc} + M(N_{pc}-N_{mc})}$$

$$= \frac{f_{in}}{MN_{mc}+N_{mc}+MN_{pc}-MN_{mc}}$$

$$= \frac{f_{in}}{MN_{pc}+N_{mc}}$$

In terms of the synthesizer application, $f_{VCO} = (MN_{pc} + N_{mc})\, f_{ref}$ and channels can be selected every f_{ref} by letting N_{pc} and N_{mc} take on suitable integer values, including zero.

A simplified example of this technique is shown in Figure 6. The MC12012 Dual Modulus Prescaler divides by either 10 or 11 when connected as shown in Figure 6. If the E3 and E4 Enable inputs are high at the start of a prescaler cycle, division by 10 results; if the Enable inputs are low at the beginning of the cycle, division by 11 results. The zero detection circuitry of the MC12014 Counter Control Logic is connected to monitor the outputs of the modulus control counter; this provides a suitable enable signal at E0 as the modulus control counter reaches its terminal (zero) count. The remainder of the MC12014 is connected to extend the operating frequency of the programmable counter chain. Appropriate waveforms for division by 43 are shown in Figure 7a.

The beginning of the timing diagram indicates circuit status just prior to the end of a countdown cycle, i.e., the modulus control counter has been counted down to one and the programmable counter is in the two state. The next positive transition from the prescaler (f1 in the timing diagram) then initiates the following sequence of events. Since the two state of the programmable counter enables the early decode circuitry in the MC12014, the positive f1 transition causes f_{out} to go low. Since f_{out} is connected to the Parallel Enables of all the MC74416 counters this low signal will re-program the counters in readiness for another cycle. However, due to the propagation time through the decode circuitry, the programmable and modulus control counters are briefly decremented to one and zero, respectively, before re-programming occurs. The momentary zero state of the modulus control counter is detected, setting E_O of the MC12014 high, enabling the MC12012 for division by ten during its next cycle. After eleven more f_{in} pulses (E_O went high after the beginning of the prescaler cycle and so doesn't change the modulus until the next prescaler cycle), f1 again goes high, causing f_{out} to return to the one state. This releases the Parallel Enables and simultaneously resets E_O to zero. However, since E_O was high when the current prescaler cycle began, the next positive f1 transition occurs only ten f_{in} pulses later. Subsequent f1 transitions now decrement the MC4016 counters down through another cycle with the prescaler dividing by eleven. From the waveforms, 11 + 10 + 11 + 11 = 43 input pulses occur for each output pulse.

Division by 42 is shown in Figure 7b. Operation is similar except that the modulus control counter reaches its terminal count one f1 cycle earlier than before. Since

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FIGURE 6 – FREQUENCY DIVISION: $f_O = f_{in}/(MN_{pc} + N_{mc})$

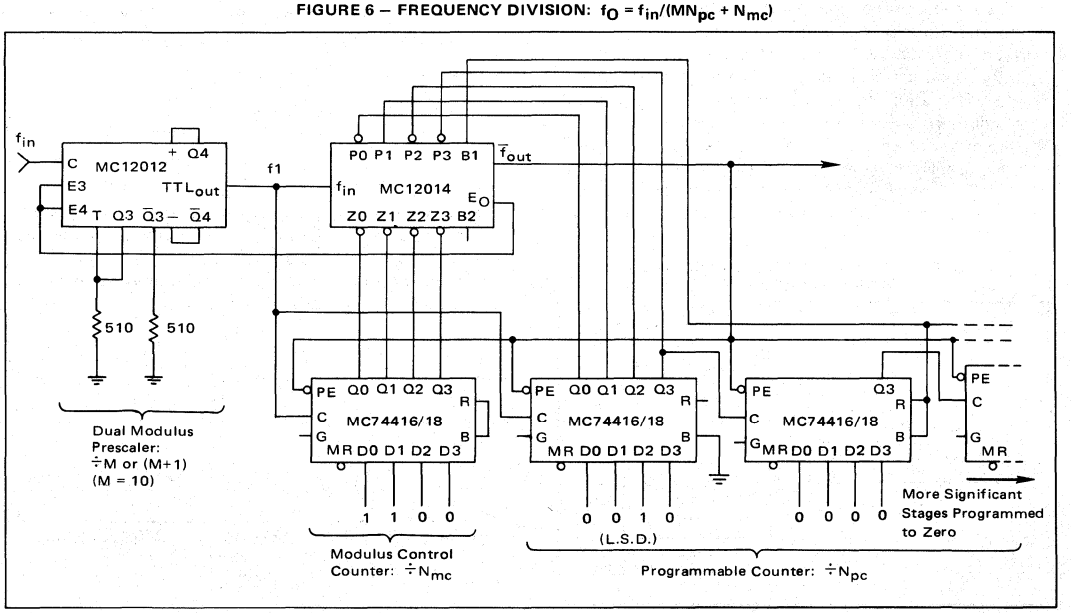


FIGURE 7a – DIVISION BY 43

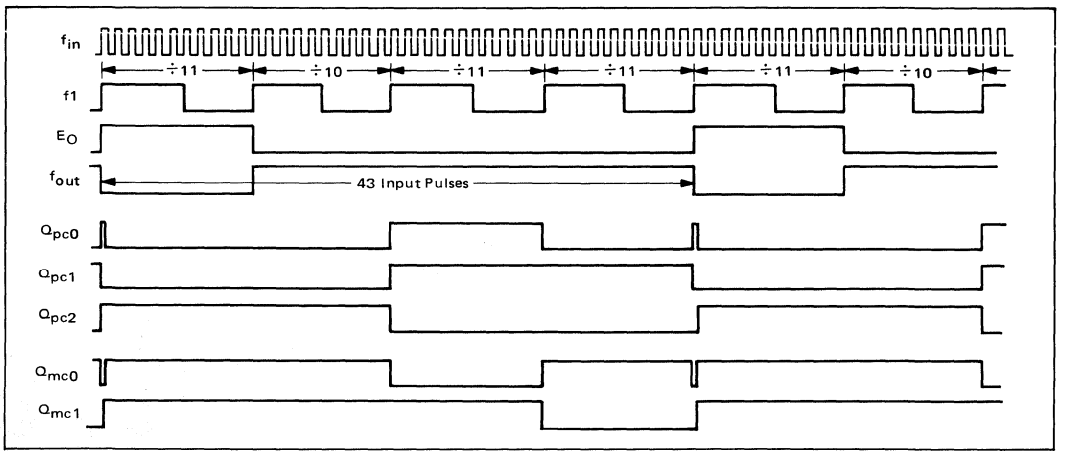
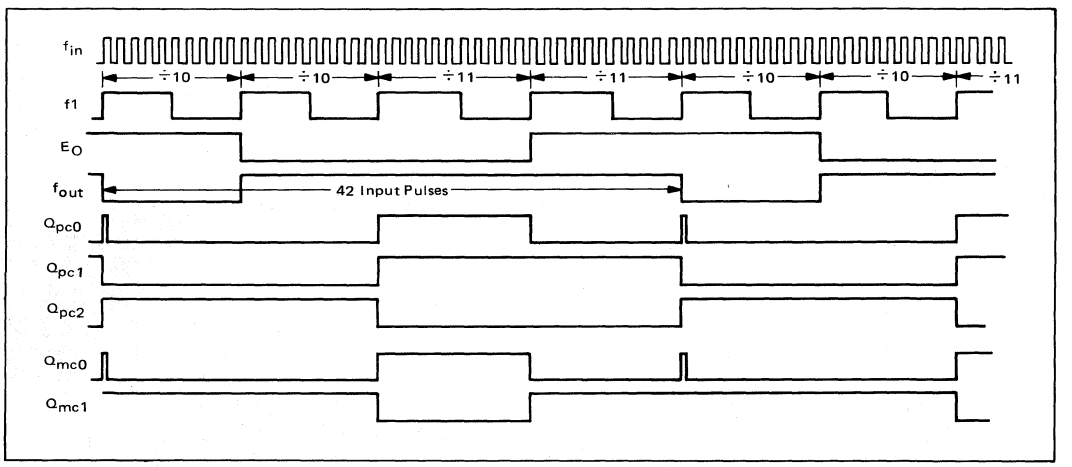


FIGURE 7b – DIVISION BY 42



E_O is reset by the trailing edge of the f_{out} pulse, E_O now remains high for two prescaler cycles leading to 10 + 10 + 11 + 11 = 42 input pulses for each output pulse.

Other combinations lead to similar results, however note that N_{pc} must be greater than or equal to N_{mc} for operation as described. If N_{mc} is greater than N_{pc} erroneous results are obtained, however this is not a serious restriction since N_{pc} is greater than N_{mc} in most practical applications.

The synthesizer shown in Figure 8 generates frequencies in the range from 144 to 178 MHz with 30 kHz channel spacing. It uses the dual modulus prescaler approach discussed earlier. General synthesizer design considerations are detailed in the publications listed in footnote 2, hence only the feedback counter is discussed here. Requirements for the feedback divider are determined from:

$$\text{Minimum Divider Ratio} = N_{Tmin} = \frac{144.00\ \text{MHz}}{30\ \text{kHz}} = 4800$$

$$\text{Maximum Divider Ratio} = N_{Tmax} = \frac{177.99\ \text{MHz}}{30\ \text{kHz}} = 5933$$

If the prescaler divides by at least ten, the maximum input frequency to the TTL counters will be 17.799 MHz, allowing use of MC74416 Programmable Counters with the MC12014 frequency extension feature.

FIGURE 8 – 144 TO 178 MHz FREQUENCY SYNTHESIZER WITH 30 kHz CHANNEL SPACING

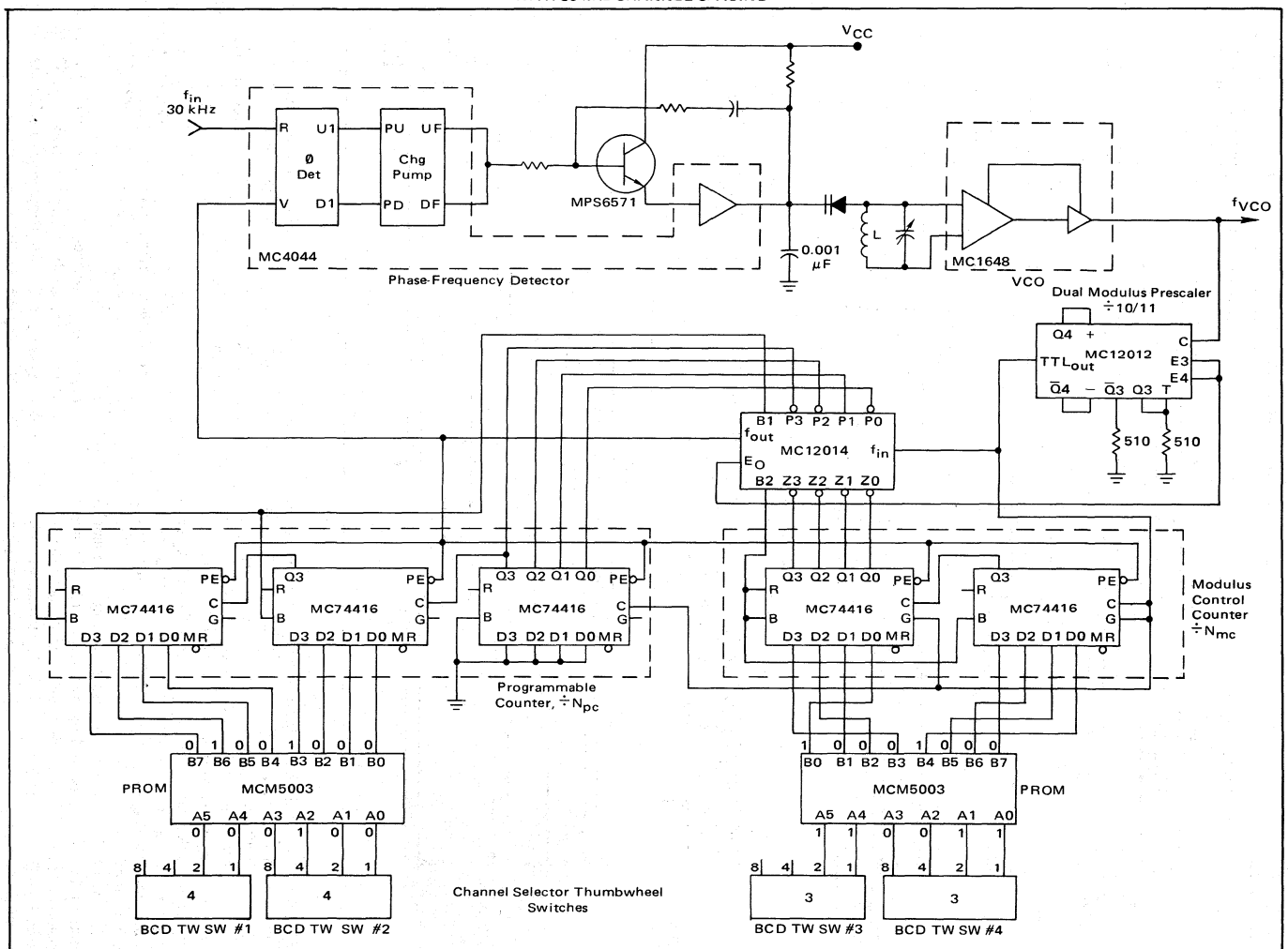


FIGURE 9 – N_{pc} PROM PROGRAMMING

	SW #1	SW #2	SW #1 A5 A4	SW #2 A3 A2 A1 A0	PROM WORD	PROM OUTPUT M.S.B.	PROM OUTPUT L.S.B.	N_{pc}	
(144 MHz)	44		0 1 0 0	0 1 0 0	4	0 1 0 0	1 0 0 0	48	480
	45		0 1 0 0	0 1 0 1	5	0 1 0 0	1 0 0 0	48	
	46		0 1 0 0	0 1 1 0	6	0 1 0 0	1 0 0 0	48	
	47		0 1 0 0	0 1 1 1	7	0 1 0 0	1 0 0 1	49	
	48		0 1 0 0	1 0 0 0	8	0 1 0 0	1 0 0 1	49	
	49		0 1 0 0	1 0 0 1	9	0 1 0 0	1 0 0 1	49	
	50		0 1 0 1	0 0 0 0	16	0 1 0 1	0 0 0 0	50	
	51		0 1 0 1	0 0 0 1	17	0 1 0 1	0 0 0 0	50	
	52		0 1 0 1	0 0 1 0	18	0 1 0 1	0 0 0 0	50	
	53		0 1 0 1	0 0 1 1	19	0 1 0 1	0 0 0 1	51	
	54		0 1 0 1	0 1 0 0	20	0 1 0 1	0 0 0 1	51	
	55		0 1 0 1	0 1 0 1	21	0 1 0 1	0 0 0 1	51	
	56		0 1 0 1	0 1 1 0	22	0 1 0 1	0 0 1 0	52	
	57		0 1 0 1	0 1 1 1	23	0 1 0 1	0 0 1 0	52	
	58		0 1 0 1	1 0 0 0	24	0 1 0 1	0 0 1 0	52	
	59		0 1 0 1	1 0 0 1	25	0 1 0 1	0 0 1 1	53	
	60		0 1 1 0	0 0 0 0	32	0 1 0 1	0 0 1 1	53	
	61		0 1 1 0	0 0 0 1	33	0 1 0 1	0 0 1 1	53	
	62		0 1 1 0	0 0 1 0	34	0 1 0 1	0 1 0 0	54	
	63		0 1 1 0	0 0 1 1	35	0 1 0 1	0 1 0 0	54	
	64		0 1 1 0	0 1 0 0	36	0 1 0 1	0 1 0 0	54	
	65		0 1 1 0	0 1 0 1	37	0 1 0 1	0 1 0 1	55	
	66		0 1 1 0	0 1 1 0	38	0 1 0 1	0 1 0 1	55	
	67		0 1 1 0	0 1 1 1	39	0 1 0 1	0 1 0 1	55	
	68		0 1 1 0	1 0 0 0	40	0 1 0 1	0 1 1 0	56	
	69		0 1 1 0	1 0 0 1	41	0 1 0 1	0 1 1 0	56	
	70		0 1 1 1	0 0 0 0	48	0 1 0 1	0 1 1 0	56	
	71		0 1 1 1	0 0 0 1	49	0 1 0 1	0 1 1 1	57	
	72		0 1 1 1	0 0 1 0	50	0 1 0 1	0 1 1 1	57	
	73		0 1 1 1	0 0 1 1	51	0 1 0 1	0 1 1 1	57	
	74		0 1 1 1	0 1 0 0	52	0 1 0 1	1 0 0 0	58	
	75		0 1 1 1	0 1 0 1	53	0 1 0 1	1 0 0 0	58	
	76		0 1 1 1	0 1 1 0	54	0 1 0 1	1 0 0 0	58	
(177 MHz)	77		0 1 1 1	0 1 1 1	55	0 1 0 1	1 0 0 1	59	590

WORD	BIT 7	6	5	4	3	2	1	0
0	–	–	–	–	–	–	–	–
1	–	–	–	–	–	–	–	–
2	–	–	–	–	–	–	–	–
3	–	–	–	–	–	–	–	–
4	0	1	0	0	1	0	0	0
5	0	1	0	0	1	0	0	0
6	0	1	0	0	1	0	0	0
7	0	1	0	0	1	0	0	1
8	0	1	0	0	1	0	0	1
9	0	1	0	0	1	0	0	1
10	–	–	–	–	–	–	–	–
11	–	–	–	–	–	–	–	–
12	–	–	–	–	–	–	–	–
13	–	–	–	–	–	–	–	–
14	–	–	–	–	–	–	–	–
15	–	–	–	–	–	–	–	–
16	0	1	0	1	0	0	0	0
17	0	1	0	1	0	0	0	0
18	0	1	0	1	0	0	0	0
19	0	1	0	1	0	0	0	1
20	0	1	0	1	0	0	0	1
21	0	1	0	1	0	0	0	1
22	0	1	0	1	0	0	1	0
23	0	1	0	1	0	0	1	0
24	0	1	0	1	0	0	1	0
25	0	1	0	1	0	0	1	1
26	–	–	–	–	–	–	–	–
27	–	–	–	–	–	–	–	–
28	–	–	–	–	–	–	–	–
29	–	–	–	–	–	–	–	–
30	–	–	–	–	–	–	–	–
31	–	–	–	–	–	–	–	–
32	0	1	0	1	0	0	1	1
33	0	1	0	1	0	0	1	1
34	0	1	0	1	0	1	0	0
35	0	1	0	1	0	1	0	0
36	0	1	0	1	0	1	0	0
37	0	1	0	1	0	1	0	1
38	0	1	0	1	0	1	0	1
39	0	1	0	1	0	1	0	1
40	0	1	0	1	0	1	1	0
41	0	1	0	1	0	1	1	0
42	–	–	–	–	–	–	–	–
43	–	–	–	–	–	–	–	–
44	–	–	–	–	–	–	–	–
45	–	–	–	–	–	–	–	–
46	–	–	–	–	–	–	–	–
47	–	–	–	–	–	–	–	–
48	0	1	0	1	0	1	1	0
49	0	1	0	1	0	1	1	1
50	0	1	0	1	0	1	1	1
51	0	1	0	1	0	1	1	1
52	0	1	0	1	1	0	0	0
53	0	1	0	1	1	0	0	0
54	0	1	0	1	1	0	0	0
55	0	1	0	1	1	0	0	1
56	–	–	–	–	–	–	–	–
57	–	–	–	–	–	–	–	–
58	–	–	–	–	–	–	–	–
59	–	–	–	–	–	–	–	–
60	–	–	–	–	–	–	–	–
61	–	–	–	–	–	–	–	–
62	–	–	–	–	–	–	–	–
63	–	–	–	–	–	–	–	–

The required divider range, 4800 to 5933, is obtained in the following manner: the MC12012 Dual Modulus Prescaler is connected in the divide by 10/11 mode; the modulus control counter uses two MC74416 stages with N_{mc} ranging from 00 to 99, establishing the two least significant digits of N_T. The remaining two digits of N_T are obtained from a three stage programmable counter generating N_{pc}. The least significant stage of the N_{pc} counter is fixed programmed to zero. The required programming for all remaining stages is derived from four channel selector BCD thumbwheel switches. The relationship between N_T and the counters is given by $N_T = MN_{pc} + N_{mc}$; for a typical channel, say 144.33 MHz, N_T = 4811 requires that M = 10, N_{pc} = 480, and N_{mc} = 11, or N_T = (10)(480) + 11 = 4811.

A general problem associated with synthesizer design arises from the fact that there is not always a one-to-one correspondence between the code provided by the channel selector switches and the code required for proper programming of the counters. For instance, in the example above where 144.33 MHz was selected, the channel selector switches are set to 44.33 while the required divider ratio is 4811. There are numerous solutions for a given translation requirement, however the method shown here using read only memories offers a straight-forward design method. While field programmable read only memories (PROMs)[3] are shown, they would normally be used only during development; suitable fixed ROMs are more economical in production quantities. The design procedure for the code conversion is illustrated in Figure 9. The required pro-

3 See the MCM5003 data sheet and AN-550 for details of operation; briefly, one of 64 eight-bit output words is selected by a six-bit address applied to the input. The word located at each address can be field programmed by the user.

FIGURE 10 – N_{mc} PROM # 1 PROGRAMMING

	SW #3	SW #4	SW #3	SW #4	PROM	PROM OUTPUT		
			A5 A4	A3 A2 A1 A0	WORD	M.S.B	L.S.B.	N_{mc}
(144)	.00		0 0 0 0	0 0 0 0	0	0 0 0 0	0 0 0 0	00
	.03		0 0 0 0	0 0 1 1	3	0 0 0 0	0 0 0 1	01
	.06		0 0 0 0	0 1 1 0	6	0 0 0 0	0 0 1 0	02
	.09		0 0 0 0	1 0 0 1	9	0 0 0 0	0 0 1 1	03
	.12		0 0 0 1	0 0 1 0	18	0 0 0 0	0 1 0 0	04
	.15		0 0 0 1	0 1 0 1	21	0 0 0 0	0 1 0 1	05
	.18		0 0 0 1	1 0 0 0	24	0 0 0 0	0 1 1 0	06
	.21		0 0 1 0	0 0 0 1	33	0 0 0 0	0 1 1 1	07
	.24		0 0 1 0	0 1 0 0	36	0 0 0 0	1 0 0 0	08
	.27		0 0 1 0	0 1 1 1	39	0 0 0 0	1 0 0 1	09
	.30		0 0 1 1	0 0 0 0	48	0 0 0 1	0 0 0 0	10
	.33		0 0 1 1	0 0 1 1	51	0 0 0 1	0 0 0 1	11
	.36		0 0 1 1	0 1 1 0	54	0 0 0 1	0 0 1 0	12
	.39		0 0 1 1	1 0 0 1	57	0 0 0 1	0 0 1 1	13
	.42		0 1 0 0	0 0 1 0	2	0 0 0 1	0 1 0 0	14
	.45		0 1 0 0	0 1 0 1	5	0 0 0 1	0 1 0 1	15
	.48		0 1 0 0	1 0 0 0	8	0 0 0 1	0 1 1 0	16
	.51		0 1 0 1	0 0 0 1	17	0 0 0 1	0 1 1 1	17
	.54		0 1 0 1	0 1 0 0	20	0 0 0 1	1 0 0 0	18
	.57		0 1 0 1	0 1 1 1	23	0 0 0 1	1 0 0 1	19
	.60		0 1 1 0	0 0 0 0	32	0 0 1 0	0 0 0 0	20
	.63		0 1 1 0	0 0 1 1	35	0 0 1 0	0 0 0 1	21
	.66		0 1 1 0	0 1 1 0	38	0 0 1 0	0 0 1 0	22
	.69		0 1 1 0	1 0 0 1	41	0 0 1 0	0 0 1 1	23
	.72		0 1 1 1	0 0 1 0	49	0 0 1 0	0 1 0 0	24
	.75		0 1 1 1	0 1 0 1	53	0 0 1 0	0 1 0 1	25
	.78		0 1 1 1	1 0 0 0	56	0 0 1 0	0 1 1 0	26
	.81		1 0 0 0	0 0 0 1	1	0 0 1 0	0 1 1 1	27
	.84		1 0 0 0	0 1 0 0	4	0 0 1 0	1 0 0 0	28
	.87		1 0 0 0	0 1 1 1	7	0 0 1 0	1 0 0 1	29
	.90		1 0 0 1	0 0 0 0	16	0 0 1 1	0 0 0 0	30
	.93		1 0 0 1	0 0 1 1	19	0 0 1 1	0 0 0 1	31
	.96		1 0 0 1	0 1 1 0	22	0 0 1 1	0 0 1 0	32
(144)	.99		1 0 0 1	1 0 0 1	25	0 0 1 1	0 0 1 1	33

Use with frequency ranges:

144.00 – 144.99	162.00 – 162.99
147.00 – 147.99	165.00 – 165.99
150.00 – 150.99	168.00 – 168.99
153.00 – 153.99	171.00 – 171.99
156.00 – 156.99	174.00 – 174.99
159.00 – 159.99	177.00 – 177.99

	BIT							
WORD	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	1	1	1
2	0	0	0	1	0	1	0	0
3	0	0	0	0	0	0	0	1
4	0	0	1	0	1	0	0	0
5	0	0	0	1	0	1	0	1
6	0	0	0	0	0	0	1	0
7	0	0	1	0	1	0	0	1
8	0	0	0	1	0	1	1	0
9	0	0	0	0	0	0	1	1
10	–	–	–	–	–	–	–	–
11	–	–	–	–	–	–	–	–
12	–	–	–	–	–	–	–	–
13	–	–	–	–	–	–	–	–
14	–	–	–	–	–	–	–	–
15	–	–	–	–	–	–	–	–
16	0	0	1	1	0	0	0	0
17	0	0	0	1	0	1	1	1
18	0	0	0	0	0	1	0	0
19	0	0	1	1	0	0	0	1
20	0	0	0	1	1	0	0	0
21	0	0	0	0	0	1	0	1
22	0	0	1	1	0	0	1	0
23	0	0	0	1	1	0	0	1
24	0	0	0	0	0	1	1	0
25	0	0	1	1	0	0	1	1
26	–	–	–	–	–	–	–	–
27	–	–	–	–	–	–	–	–
28	–	–	–	–	–	–	–	–
29	–	–	–	–	–	–	–	–
30	–	–	–	–	–	–	–	–
31	–	–	–	–	–	–	–	–
32	0	0	1	0	0	0	0	0
33	0	0	0	0	0	1	1	1
34	–	–	–	–	–	–	–	–
35	0	0	1	0	0	0	0	1
36	0	0	0	0	1	0	0	0
37	–	–	–	–	–	–	–	–
38	0	0	1	0	0	0	1	0
39	0	0	0	0	1	0	0	1
40	–	–	–	–	–	–	–	–
41	0	0	1	0	0	0	1	1
42	–	–	–	–	–	–	–	–
43	–	–	–	–	–	–	–	–
44	–	–	–	–	–	–	–	–
45	–	–	–	–	–	–	–	–
46	–	–	–	–	–	–	–	–
47	–	–	–	–	–	–	–	–
48	0	0	0	1	0	0	0	0
49	0	0	1	0	0	1	0	0
50	–	–	–	–	–	–	–	–
51	0	0	0	1	0	0	0	1
52	–	–	–	–	–	–	–	–
53	0	0	1	0	0	1	0	1
54	0	0	0	1	0	0	1	0
55	–	–	–	–	–	–	–	–
56	0	0	1	0	0	1	1	0
57	0	0	0	1	0	0	1	1
58	–	–	–	–	–	–	–	–
59	–	–	–	–	–	–	–	–
60	–	–	–	–	–	–	–	–
61	–	–	–	–	–	–	–	–
62	–	–	–	–	–	–	–	–
63	–	–	–	–	–	–	–	–

5

gramming for the two most significant digits of N_{pc} is shown versus the code provided by switches #1 and #2 of the channel selector. If the four outputs of switch #2 and the two least significant outputs of switch #1 are regarded as address bits A0 through A5 for an MCM5003 PROM, a memory location can be associated with each switch setting. The required N_{pc} programming for each switch setting is then set into the appropriate memory location by the user. In Figure 9, the required programming has been transferred into a truth table to be used while programming the PROM. A similar result for the N_{mc} programming is shown in Figure 10. Note that the PROM shown, N_{mc} PROM #1, selects only N_{mc} numbers 00 through 33. This means that the synthesizer as shown in Figure 8 selects only the adjacent channels in a one megahertz slice of the total band. The frequency ranges that can be selected using N_{mc} PROM #1 are summarized in Figure 10. For other ranges, N_{mc} PROM #1 must be replaced by one of two additional PROMs required for generating the remaining N_{mc} numbers. Appropriate truth tables along with the ranges they can be used with are shown in Figures 11 and 12.

FIGURE 11 – N_{mc} PROM #2 TRUTH TABLE

WORD	BIT 7	6	5	4	3	2	1	0
0	0	1	1	0	0	0	0	0
1	0	1	0	0	0	1	1	1
2	0	0	1	1	0	1	0	0
3	0	1	1	0	0	0	0	1
4	0	1	0	0	1	0	0	0
5	0	0	1	1	0	1	0	1
6	0	1	1	0	0	0	1	0
7	0	1	0	0	1	0	0	1
8	0	0	1	1	0	1	1	0
9	0	1	1	0	0	0	1	1
10	–	–	–	–	–	–	–	–
11	–	–	–	–	–	–	–	–
12	–	–	–	–	–	–	–	–
13	–	–	–	–	–	–	–	–
14	–	–	–	–	–	–	–	–
15	–	–	–	–	–	–	–	–
16	0	1	0	1	0	0	0	0
17	0	0	1	1	0	1	1	1
18	0	1	1	0	0	1	0	0
19	0	1	0	1	0	0	0	1
20	0	0	1	1	1	0	0	0
21	0	1	1	0	0	1	0	1
22	0	1	0	1	0	0	1	0
23	0	0	1	1	1	0	0	1
24	0	1	1	0	0	1	1	0
25	0	1	0	1	0	0	1	1
26	–	–	–	–	–	–	–	–
27	–	–	–	–	–	–	–	–
28	–	–	–	–	–	–	–	–
29	–	–	–	–	–	–	–	–
30	–	–	–	–	–	–	–	–
31	–	–	–	–	–	–	–	–
32	0	1	0	0	0	0	0	0
33	–	–	–	–	–	–	–	–
34	0	1	0	1	0	1	0	0
35	0	1	0	0	0	0	0	1
36	–	–	–	–	–	–	–	–
37	0	1	0	1	0	1	0	1
38	0	1	0	0	0	0	1	0
39	–	–	–	–	–	–	–	–
40	0	1	0	1	0	1	1	0
41	0	1	0	0	0	0	1	1
42	–	–	–	–	–	–	–	–
43	–	–	–	–	–	–	–	–
44	–	–	–	–	–	–	–	–
45	–	–	–	–	–	–	–	–
46	–	–	–	–	–	–	–	–
47	–	–	–	–	–	–	–	–
48	–	–	–	–	–	–	–	–
49	0	1	0	1	0	1	1	1
50	0	1	0	0	0	1	0	0
51	–	–	–	–	–	–	–	–
52	0	1	0	1	1	0	0	0
53	0	1	0	0	0	1	0	1
54	–	–	–	–	–	–	–	–
55	0	1	0	1	1	0	0	1
56	0	1	0	0	0	1	1	0
57	–	–	–	–	–	–	–	–
58	–	–	–	–	–	–	–	–
59	–	–	–	–	–	–	–	–
60	–	–	–	–	–	–	–	–
61	–	–	–	–	–	–	–	–
62	–	–	–	–	–	–	–	–
63	–	–	–	–	–	–	–	–

Use with frequency ranges:

145.02 – 145.98
148.02 – 148.98
151.02 – 151.98
154.02 – 154.98
157.02 – 157.98
160.02 – 160.98
163.02 – 163.98
166.02 – 166.98
169.02 – 169.98
172.02 – 172.98
175.02 – 175.98

FIGURE 12 – N_{mc} PROM #3 TRUTH TABLE

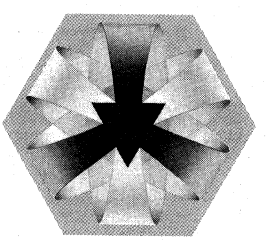
WORD	BIT 7	6	5	4	3	2	1	0
0	1	0	0	0	0	0	0	0
1	0	1	1	0	0	1	1	1
2	1	0	0	1	0	1	0	0
3	1	0	0	0	0	0	0	1
4	0	1	1	0	1	0	0	0
5	1	0	0	1	0	1	0	1
6	1	0	0	0	0	0	1	0
7	0	1	1	0	1	0	0	1
8	1	0	0	1	0	1	1	0
9	1	0	0	0	0	0	1	1
10	–	–	–	–	–	–	–	–
11	–	–	–	–	–	–	–	–
12	–	–	–	–	–	–	–	–
13	–	–	–	–	–	–	–	–
14	–	–	–	–	–	–	–	–
15	–	–	–	–	–	–	–	–
16	0	1	1	1	0	0	0	0
17	1	0	0	1	0	1	1	1
18	1	0	0	0	0	1	0	0
19	0	1	1	1	0	0	0	1
20	1	0	0	1	1	0	0	0
21	1	0	0	0	0	1	0	1
22	0	1	1	1	0	0	1	0
23	1	0	0	1	1	0	0	1
24	1	0	0	0	0	1	1	0
25	0	1	1	1	0	0	1	1
26	–	–	–	–	–	–	–	–
27	–	–	–	–	–	–	–	–
28	–	–	–	–	–	–	–	–
29	–	–	–	–	–	–	–	–
30	–	–	–	–	–	–	–	–
31	–	–	–	–	–	–	–	–
32	–	–	–	–	–	–	–	–
33	1	0	0	0	0	1	1	1
34	0	1	1	1	0	1	0	0
35	–	–	–	–	–	–	–	–
36	–	–	–	–	–	–	–	–
37	0	1	1	1	0	1	0	1
38	1	0	0	0	1	0	0	0
39	1	0	0	0	1	0	0	1
40	0	1	1	1	0	1	1	0
41	–	–	–	–	–	–	–	–
42	–	–	–	–	–	–	–	–
43	–	–	–	–	–	–	–	–
44	–	–	–	–	–	–	–	–
45	–	–	–	–	–	–	–	–
46	–	–	–	–	–	–	–	–
47	–	–	–	–	–	–	–	–
48	1	0	0	1	0	0	0	0
49	0	1	1	1	0	1	1	1
50	–	–	–	–	–	–	–	–
51	1	0	0	1	0	0	0	1
52	0	1	1	1	1	0	0	0
53	–	–	–	–	–	–	–	–
54	1	0	0	1	0	0	1	0
55	0	1	1	1	1	0	0	1
56	–	–	–	–	–	–	–	–
57	1	0	0	0	0	0	1	1
58	–	–	–	–	–	–	–	–
59	–	–	–	–	–	–	–	–
60	–	–	–	–	–	–	–	–
61	–	–	–	–	–	–	–	–
62	–	–	–	–	–	–	–	–
63	–	–	–	–	–	–	–	–

Use with frequency ranges:

146.01 – 146.97
149.01 – 149.97
152.01 – 152.97
155.01 – 155.97
158.01 – 158.97
161.01 – 161.97
164.01 – 164.97
167.01 – 167.97
170.01 – 170.97
173.01 – 173.97
176.01 – 176.97

APPLICATIONS

6



AN-532A

MTTL AND MECL AVIONICS DIGITAL FREQUENCY SYNTHESIZER

Prepared by
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Applications Engineering

INTRODUCTION

Initial design of frequency synthesizers used a method of crystal switching combined with mixing to provide the multi-channel operation required. With the advent of suitable low cost digital integrated circuits, future designs of frequency synthesizers will begin to incorporate such devices for channel selection.

The basic technique used with integrated circuits is one of a digital phaselock closed loop. Inserted within the feedback loop is a programmable digital divider to provide the multi-channel capability required for avionic communications. This provides that with only one crystal reference source all the channel requirements can be generated for both the transmit and receive mode of operation. The design presented covers 118 MHz to 136 MHz, with 360 channels in 50 kHz steps. The design data included may be used to design 720 channel operation in 25 kHz steps.

The illustrations provided represent various ways that the phaselocked loop may be implemented. Any one or combinations of these techniques may yield the method a designer requires for his specific application.

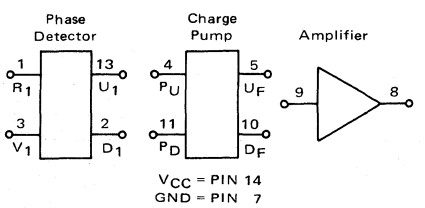

FIGURE 1 – MC4044 Block Diagram

THE MC4044 INTEGRATED CIRCUIT PHASE DETECTOR

The phase detector used in this design is a digital frequency/phase detector which includes a digital-to-analog charge pump section. Within this section is a Darlington pair of transistors that is used to form an amplifier for use as an active loop filter.

The block diagram of the MC4044, Figure 1, shows these three sections of the phase detector.[5] Figure 2 illustrates the logic/circuit diagram of the digital-analog sections. Two jumpers must be provided between the digital and analog sections. The U1 output connects to the P_U input and the D1 output connects to the P_D input. Other external connections must be made to the Darlington amplifier to incorporate the filter element of the charge pump.

The lag filter as illustrated in the shaded portion of Figure 2 is comprised of elements R1, R2, and C. A high-β transistor Q1 (MPS6571) is used to further improve the impedance level that capacitor C looks into. This significantly reduces the current leakage from the capacitor to the VCO input, which reduces loop noise level.

The MC4044 phase detector, being of TTL construction, must be well bypassed or power-supply decoupled from the rest of the system to prevent current spikes from influencing the VCO control voltage. The rest of the system that should be power supply decoupled includes the active filter amplifier's V_{CC} line and the VCO's supply line. The values selected for R1, R2 and C will depend upon closed loop performance required by the designer. In a later section the complete closed loop will be analyzed with solutions for R1, R2, and C.

MC1648 EMITTER COUPLED OSCILLATOR

The voltage controlled oscillator illustrated in Figure 3 is an ECL tuned inductor type oscillator utilizing a MECL III emitter coupled oscillator (MC1648) and an Epicap (MV1404) hyper-abrupt junction tuning diode.[6,7,8] The tuned circuit elements should have as high a loaded Q as possible to provide good output spectral purity. Good VHF RF layout techniques should be used, with all voltage inputs RF decoupled. Because of the operation of TTL within the system with its associated high di/dt content, the bypassing should include not only VHF but also low frequency filtering. Most susceptible to coupling are the filter amplifier V_{CC}, the ECO bias point, the ECO AGC point, and the ECO V_{EE} points. It is also recommended that the sinewave output of the VCO be buffered before external use. The actual step-by-step design of an Epicap tuned VCO is beyong the intent of this note, however excellent reference material is available in AN-178A. As discussed in the section on programmable counter operation, the VCO should tune between 117.3 MHz and 138.65 MHz.

The design should include a guard-band at each end of the range such that the VCO tunes from 110 MHz to 145 MHz. The lower control voltage has a minimum value of 1.8 volts at 110 MHz and an upper voltage of 5 volts at 145 MHz when using a MV1404 Epicap variable voltage capacitance diode. If a larger tuning voltage for the Epicap diodes is needed, the collector supply voltage to the MC4044 filter amplifier (through a 1 k resistor) may be elevated up to a maximum of 8 volts. Still larger voltage ranges are available by using an external amplifier/filter.

The output of the MC1648 is a sinewave with proper

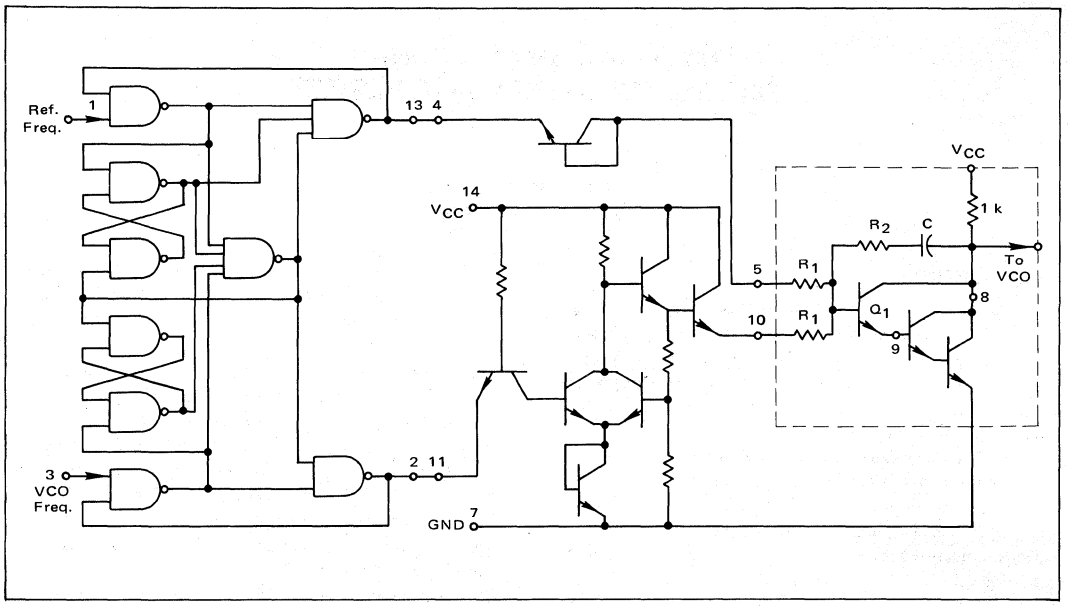

FIGURE 2 – MC4044 Logic/Circuit Diagram

peak-to-peak range to interface directly with MECL dividers. The value of this peak-to-peak swing may be changed by connecting a 5 k potentiometer between the AGC point and V_{EE}. It is important to note that the anode of the tuning diode is biased to a voltage level of about two V_{BE} diode drops above V_{EE}. This fixed bias of -3.8 volts will insure that the Epicap is always reversed biased even at zero tuning voltage. The input stray capacitance of the MC1648 ECO is C_T = 6 pF, which is a required parameter to properly design the LC tank of the ECO.

THE MECL PRESCALER

A fixed divide-by-10 prescaler is used between the VCO output and the programmable counter section. The prescaler in Figure 4 is a high speed divide-by-two MC1034 flip-flop followed by a divide-by-five section using a MC1032 and MC1027.[4] For operation at temperatures between -55°C and +125°C the counter should employ an MC1234L followed by three MC1227L flip-flops.

The MECL prescaler is operated with V_{EE} at -5.2 V and the V_{CC} terminals grounded.

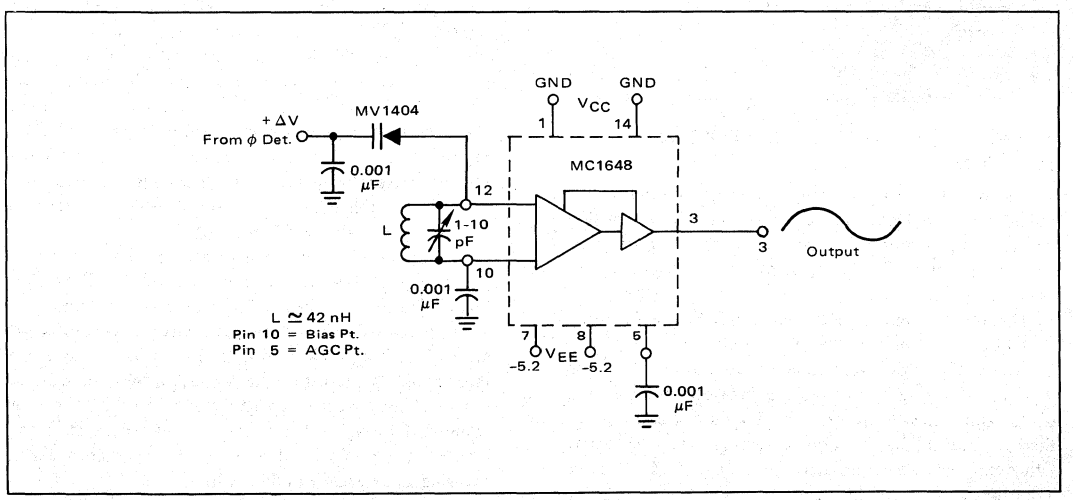

FIGURE 3 – Emitter Coupled Oscillator

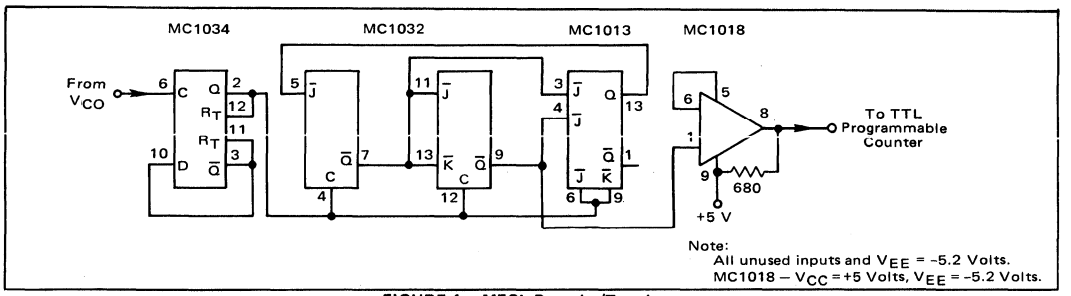

FIGURE 4 – MECL Prescaler/Translator

The output of the MECL prescaler has a maximum output frequency of 13.865 MHz. The negative voltage logic swing being between -0.75 volts and -1.6 V requires translation to provide TTL logic levels to the programmable counter section. This translation is provided by means of a MC1018 driven from the third MECL flip-flop. This prescaled function is represented by an 1/M in the phase locked loop block diagram (Figure 8), where M = 10.

ANALYSIS OF THE PROGRAMMABLE COUNTER

In the frequency synthesizer for the aircraft band, a programmable counter is inserted in the feedback loop in order to generate multiple stable output frequencies. The logic diagram in Figure 5 shows a design for a programmable counter that can be used in the transmit and receive modes of operation. An additional feature in the receive mode is the capability of automatically adding or subtracting 10.7 MHz at the output of the VCO which reduces the design difficulties for the VCO designer.

During the receive mode of operation, if high side IF injection was used then the VCO would have to cover from 118.0 MHz + 10.7 MHz to 135.95 MHz + 10.7 MHz which is from 128.7 MHz to 146.65 MHz. Also during transmit the VCO has to operate down to 118.0, so that the VCO design would have to cover from 118.0 MHz to 146.65 MHz. With this tuning range an Epicap diode VCO using low tuning voltage is difficult to design. By using high side IF injection from 118 MHz to 127.95 MHz and then switching to low side IF injection from 128 MHz to 135.95 MHz the VCO would only be required to cover a range between 117.3 MHz and 138.65 MHz. The control logic to provide the ± IF offset function is included in Figure 5. The REC+/REC- is enabled from an extra pair of wafer or switch contacts that operate in conjunction with the frequency programming switches. If the frequency programmed is 128 MHz or greater then during the RECEIVE mode of operation the VCO output is at the programmed frequency minus 10.7 MHz. Conversely if the frequency programmed is below 128 MHz the REC+ line is at a logic low level and the VCO output frequency will be the programmed frequency plus 10.7 MHz. Table I shows the relationship between the programmed frequency, and the transmit, receive plus, and receive minus count ratios at major indices.

TABLE I – Programmed Count Frequency Relationship

Programmed Frequency (MHz)	Programmed Count	VCO Output Transmit (MHz)	÷ N During Receive	VCO Output Receive (MHz)
118.00	2360	118.00	2574	128.70
118.05	2361	118.05	2575	128.75
127.95	2559	127.95	2773	138.65
128.00	2560	128.00	2346	117.30
135.95	2719	135.95	2505	125.25

The design uses three MC4016, BCD programmable down counters which interface with three thumbwheel switches with BCD outputs or with two wafer selection switches. The first wafer switch has 18 positions stepping from 18 to 36 selecting tens of megahertz and the second switch has 20 positions stepping from 00 to 95 in 50 kHz steps. The number on the thumbwheel switches could be varied from 000 to 999, but with normal operation for aircraft synthesizers the selected range lies between 360 and 719. To illustrate the operation of the counter, assume the TRANSMIT/RECEIVE switch is placed in the TRANSMIT position and the thumbwheel switches are placed in the position to read 360. The output frequency would then be equal to the input frequency divided by 2360 (the most significant digit, 2, is automatically programmed into the counter.) The output of the VCO would be 50 kHz times the setting on the thumbwheel switches (for the case illustrated this would be 50 kHz x 2360 or 118 MHz).

Although the MC4016 is a ripple-down counter, this programmable counter design is capable of operation with an input frequency in excess of 16 MHz when proper layout techniques are used. One reason for the high speed operation is the use of special decoding logic and a control flip-flop to do the actual loading.[2] This speed up technique is shown in its basic form in Figure 6. The Q output of the control flip-flop goes low for one bit time during the load operation and also inhibits one clock pulse.

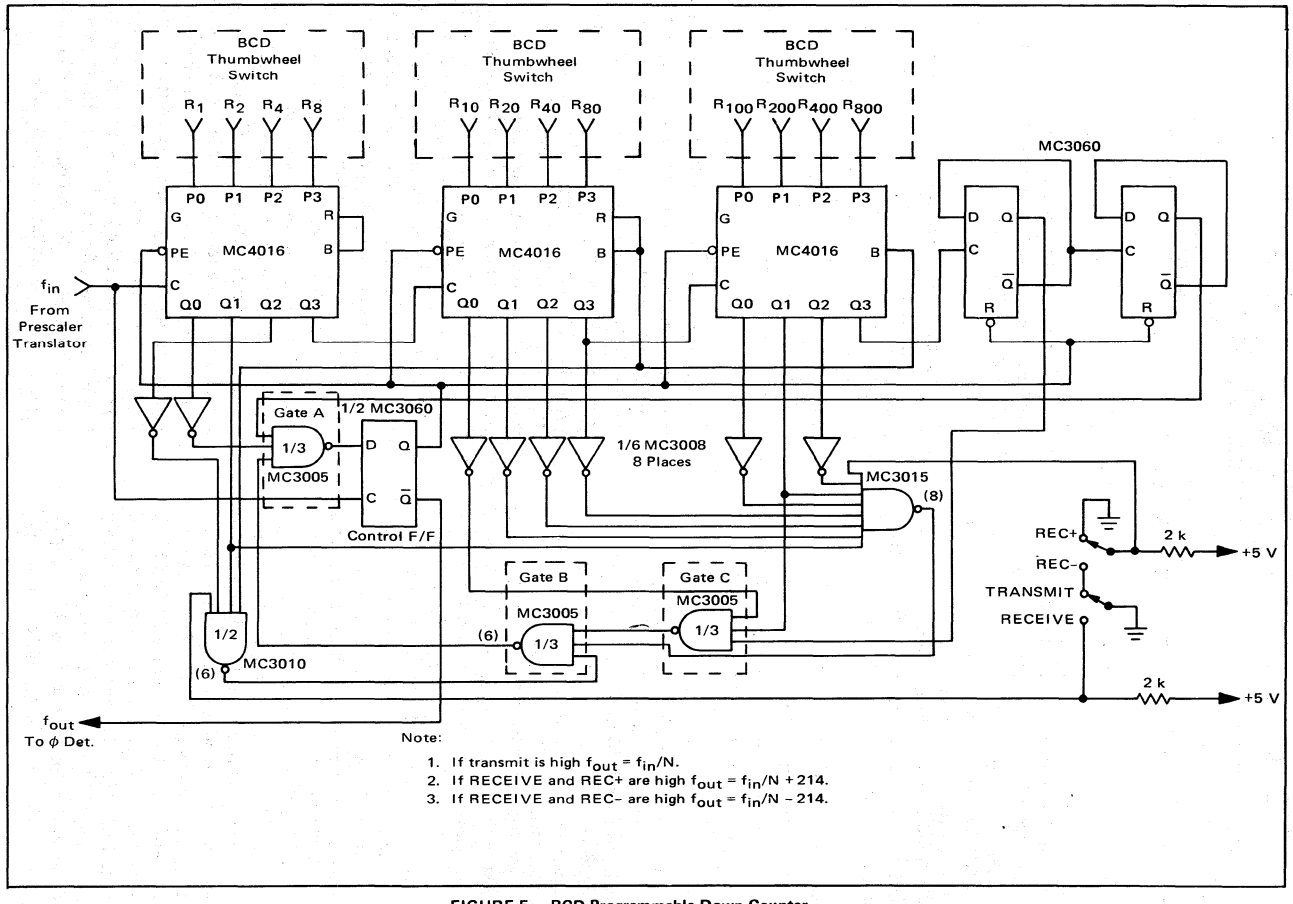

FIGURE 5 – BCD Programmable Down Counter

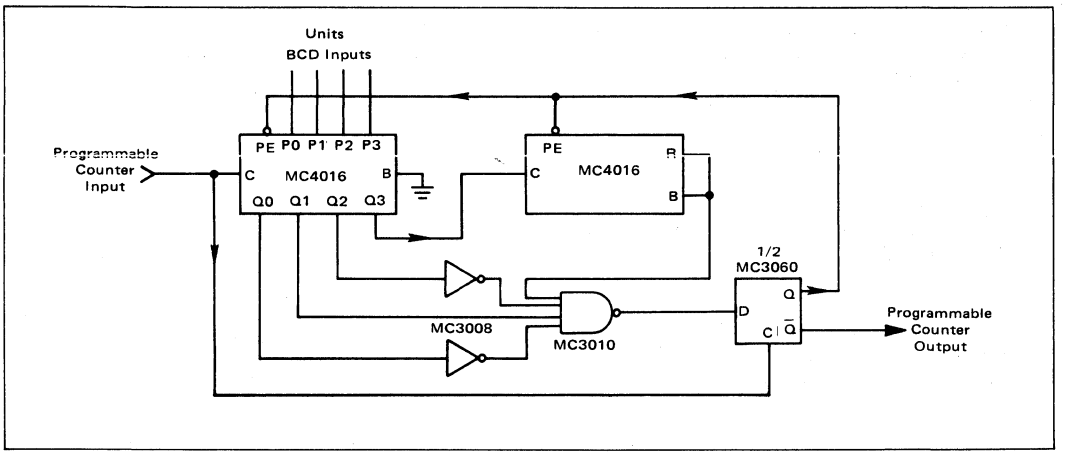

FIGURE 6 – Counter Speed-Up Technique

In the TRANSMIT mode, the output of the MC3010 (pin 6) is low and the inputs of the MC3005 (gate A in Figure 5) are high only when the counter has counted down to 002 (the most significant bits of the counter, represented by the two MC3060 flip-flops, must be in state 2). A load operation occurs in the next bit time.

Similarly, in the RECEIVE/R- position, the output of the 3015 (pin 8) is low and the inputs of gate A are high only when the counter has counted down to 216. For this case, the output frequency is equal to the input frequency divided by the number on the thumbwheel switches minus 214. For instance, if the switch setting is 2719,

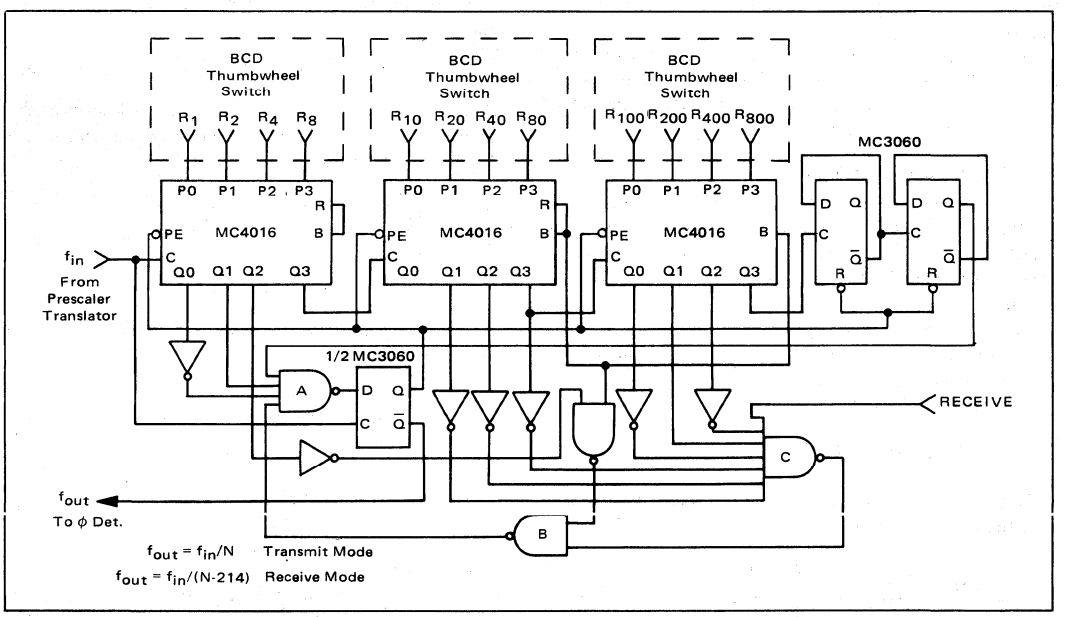

FIGURE 7 – BCD Programmable Down Counter

then the output frequency is equal to the input frequency divided by 2505 (the number 2 that is underlined, is automatically programmed into the counter.)

In the RECEIVE/R+ position, the output of the MC3005 (pin 6) is low and the inputs of gate A are high only when the counter has counted down to 788 (the most significant bits of the counter must be in state 3). Again a load operation occurs in the next bit time. The output frequency, for this case, is equal to the input frequency divided by the number on the thumbwheel switches plus 214. For instance, if the switch setting is 2360, then the output frequency is equal to the input frequency divided by 2574

The programmable counter has the following end limits. The maximum value of N is 2773 during high side receive on 127.950 MHz. The minimum value of N is 2346 during low side receive on 128.0 MHz. The value of N during the transmit mode of operation is within these limits being between 2360 and 2719.

If the ± receive IF offset feature is not required then Figure 7 illustrates the programmable counter design that places the VCO 10.7 MHz lower than the frequency selected during the transmit mode of operation.

PHASE LOCKED LOOP ANALYSIS

Consider the block diagram of the frequency synthesizer illustrated in Figure 8. The loop is composed of a phase detector, an active filter element, the VCO, a prescaled divide-by-ten counter (M), and a programmable divide-by-N counter.

First, the general equations used for loop analysis will be derived and next a specific example with a numeric solution will be solved.

Phase error is given by,

$$\theta_e(s) = \theta_i(s) - \frac{\theta_o(s)}{NM} \qquad (1)$$

Using Mason's gain rule or other methods, the closed loop transfer function is,

$$H(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{K_pK_vF(s)}{S + \frac{K_pK_vF(s)}{NM}} \qquad (2)$$

The loop filter element used in this design is an active lag type illustrated in the shaded portion of Figure 2.

The transfer function for this filter is,

$$F(s) = \frac{\tau_2 s + 1}{\tau_1 s} \qquad (3)$$

where $\tau_1 = R_1C$ and $\tau_2 = R_2C$.

Therefore, the complete closed loop transfer function is

$$H(s) = \frac{K_pK_v\left[\frac{\tau_2 s + 1}{\tau_1 s}\right]}{s^2 + \left[\frac{K_pK_v\tau_2}{\tau_1 NM}\right]s + \frac{K_pK_v}{\tau_1 NM}} \qquad (4)$$

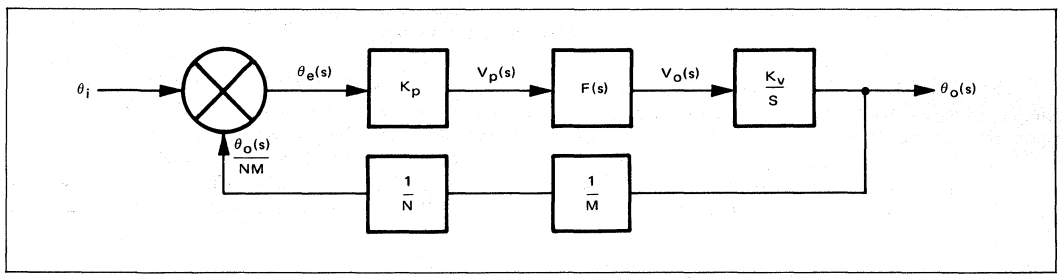

FIGURE 8 – Phase Locked Loop

The denominator of (4) takes on the form of the characteristic equation of a second-order loop from servo theory.

$$s^2 + [2\zeta\omega_n]s + \omega_n^2 \qquad (5)$$

Where ζ is the damping factor and ω_n is known as the natural loop frequency. If we plug into Equation (4) $\tau_1 = R_1C$ and $\tau_2 = R_2C$ the results are,

$$H(s) = \left[\frac{K_pK_vR_2}{R_1}\right]\frac{s + \frac{1}{R_2C}}{s^2 + \left[\frac{K_pK_vR_2}{R_1NM}\right]s + \frac{K_pK_v}{R_1CNM}} \qquad (6)$$

Comparing the denominator of Equation (6) with (5) we see that,

$$\omega_n^2 = \frac{K_pK_v}{R_1CNM} \qquad (7)$$

or

$$\omega_n = \left[\frac{K_pK_v}{R_1CNM}\right]^{1/2} \qquad (8)$$

and also that

$$\zeta = \frac{R_2C}{2}\left[\frac{K_pK_v}{R_1CNM}\right]^{1/2} \qquad (9)$$

Another useful parameter to solve for is the 3 dB bandwidth of the closed loop. By letting $s = j\omega$ in Equation (6) and setting $|H(j\omega)|^2 = 1/2$ we can obtain the bandwidth of the loop.

$$\omega_{3\,dB} = \left[-\frac{B}{2} + \left(\frac{B^2}{4} - C\right)^{1/2}\right]^{1/2} \quad (10)$$

where

$$B = \left[-\left(\frac{K_p K_v R_2}{R_1 NM}\right)^2 - \frac{2K_p K_v}{R_1 CNM}\right] \quad (11)$$

and

$$C = -\left(\frac{K_p K_v}{R_1 CNM}\right)^2 \quad (12)$$

Recalling that

$$\zeta = \frac{R_2 C}{2}\left(\frac{K_p K_v}{R_1 CNM}\right)^{1/2}$$

and

$$\omega_n = \left(\frac{K_p K_v}{R_1 CNM}\right)^{1/2}$$

we obtain

$$\omega_{3\,dB} = \omega_n\left[2\zeta^2 + 1 + \sqrt{(2\zeta^2+1)^2+1}\right]^{1/2} \quad (13)$$

Before a typical closed loop problem is solved the loop gain constants must be calculated. These being, K_p and K_V, the phase detector and voltage controlled oscillator gain constants respectively.[1,3,10]

The phase detector output voltage is proportional to the phase difference between the negative going pulse edges entering the phase detector; that is

$$V_p = K_p\,(\theta_i - \theta_o) \quad (14)$$

where K_p is the phase detector gain constant. The calculation of K_p follows from Figure 9.

Now

$$V_p = \frac{V_o\,(\theta_i - \theta_o)}{2(2\pi)} \quad (15)$$

Substituting (14) into (15)

$$K_p\,(\theta_i - \theta_o) = \frac{V_o\,(\theta_i - \theta_o)}{4\pi} \quad (16)$$

$$K_p = \frac{V_o}{4\pi} \quad (17)$$

Letting V_o equal the change in voltage at the summing junction of R_1 over a phase angle change of + or - 2π and the MC4044 operating from V_{CC} = +5 V, yields the following phase detector gain constant.

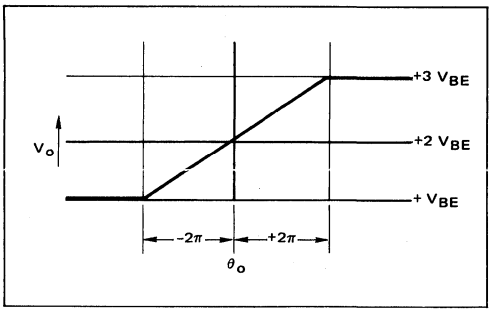

FIGURE 9 – Phase Detector Characteristic

$$K_p = \frac{2V_{BE}}{2 \times 2\pi} = \frac{0.7}{2\pi} = 0.111\ V/rad \quad (18)$$

The VCO gain constant can be calculated by knowing or measuring the VCO's change in output frequency over a change in input control voltage. As stated in an earlier section the tuning excursion of the input voltage is from 1.8 V to 5 V. Over this voltage excursion the output frequency changes by 35 MHz.

$$K_V = \frac{[(145 - 110) \times 10^6\ Hz] \times 2\pi}{(5 - 1.8)\ V}$$

$$= 6.86 \times 10^7\ rad/s/V \quad (19)$$

DESIGN CRITERIA

The loop will be designed to provide a settling time (t_S) of 28 ms. Settling time will be defined as the time required for the VCO control voltage to be within 5% of it's final value after a step change in frequency. The phase locked loop illustrated is a second-order loop with the damping factor (ζ) chosen to be 0.707. This locates the closed-loop poles at ±45 degrees off the negative real axis. The root-locus circle illustrated in Figure 10 passes through the origin of the s-plane. The poles originate at the origin

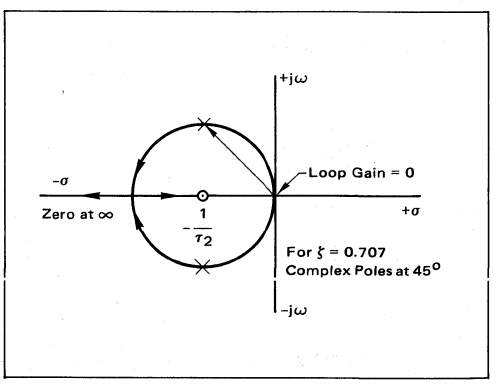

FIGURE 10 – Type II Root Locus Plot (Active Lag Filter)

when the loop gain is zero and traverse a circle with radius of $1/\tau_2$ as gain increases. With $\zeta = 0.707$ the poles are located at $1/\tau_2$ $(-1 \pm j1)$ and the zero at $-1/\tau_2$.

With the complex loop poles above and below the system zero ($\zeta = 0.707$) a peak overshoot of approximately 20% will be experienced. Knowing the peak overshoot and the requirement to be within 5% of the final value yields the following value for $\omega_n t_s = 5$. This value is extrapolated from transient response curves for second-order viscous-damped servomechanism systems when disturbed with a step-displacement input.[9] By choosing t_s = 28 ms and having determined $\omega_n t_s = 5$, then ω_n is equal to 178.

$$\omega_n = \frac{5}{28 \text{ ms}} = 178 \tag{20}$$

Recalling the characteristic Equation (5)

$$s^2 + [2\zeta\omega_n]\, s + \omega_n^2 \tag{21}$$

and the denominator of the transfer function of (6) being,

$$s^2 + \left[\frac{K_p K_v R_2}{R_1 NM}\right] s + \frac{K_p K_v}{R_1 CNM} \tag{22}$$

Then the complex roots of the characteristic Equation (21) can be broken up into real and imaginary terms,

$$(s + b)^2 + \omega^2$$

$$s^2 + 2sb + b^2 + \omega^2 \tag{23}$$

By comparing Equations (21), (22), and (23) the following equations are derived.

$$\omega_n^2 = b^2 + \omega^2 = \frac{K_p K_v}{R_1 CNM} \tag{24}$$

or

$$R_1 C = \frac{K_p K_v}{\omega_n^2 NM} \tag{25}$$

With $\zeta = 0.707$, $\quad b = \omega$

$$\therefore\ \omega_n^2 = b^2 + (b)^2 = 2b^2$$

or

$$b = \frac{1}{\sqrt{2}}\,\omega_n \tag{26}$$

Also

$$2b = \frac{K_p K_v R_2}{R_1 NM}$$

or

$$R_2 = \frac{2bR_1 NM}{K_p K_v} \tag{27}$$

Using the listed aircraft frequency synthesizer loop parameters and Equations (25) and (27) the filter values R_1, R_2 and C can be calculated.

Recalling,

$$\omega_n = 178$$

$$K_p = 1.11 \times 10^{-1} \text{ V/rad}$$

$$K_v = 6.86 \times 10^7 \text{ rad/s/V}$$

$$NM_{max} = 27730$$

$$NM_{min} = 23460$$

Substituting into (25)

$$R_1 C = \frac{(1.11 \times 10^{-1})\,(6.86 \times 10^7)}{(1.78 \times 10^2)^2 (2.773 \times 10^4)}$$

$$R_1 C = 8.6 \times 10^{-3}$$

Choose a convenient value for C that gives a realizable R_1. In this design 1 μF was chosen.

$$\therefore\ R_1 = \frac{8.6 \times 10^{-3}}{1 \times 10^{-6}} = 8.6 \text{ k}\Omega$$

R_2 may be calculated by solving Equations (26) and (27) where,

$$b = \frac{\omega_n}{\sqrt{2}} = \frac{1.78 \times 10^2}{\sqrt{2}} = 1.26 \times 10^2$$

$$\therefore\ R_2 = \frac{(2)(1.26 \times 10^2)(8.6 \times 10^3)(2.773 \times 10^4)}{(1.1 \times 10^{-1})(6.86 \times 10^7)}$$

$$R_2 = 7.8 \text{ k}\Omega$$

A circuit diagram of the complete synthesizer is shown in Figure 11. Transient response to a 1 MHz step change in frequency is shown in the computer readout of Figure 12.

SUMMARY

This report has discussed only one phaselocked loop application utilizing currently available complex digital integrated circuits. Several unique design techniques are shown that are somewhat unconventional in frequency synthesizers. Unique designs shown include: a programmable counter with arithmetic IF offset capability, such that the synthesizer can be used for both transmit and receive; a single IC digital phase detector that provides direct interface between TTL logic and the analog requirements of an emitter coupled oscillator; and a complete analysis of a phaselocked digital loop in both general terms and with a specific example.

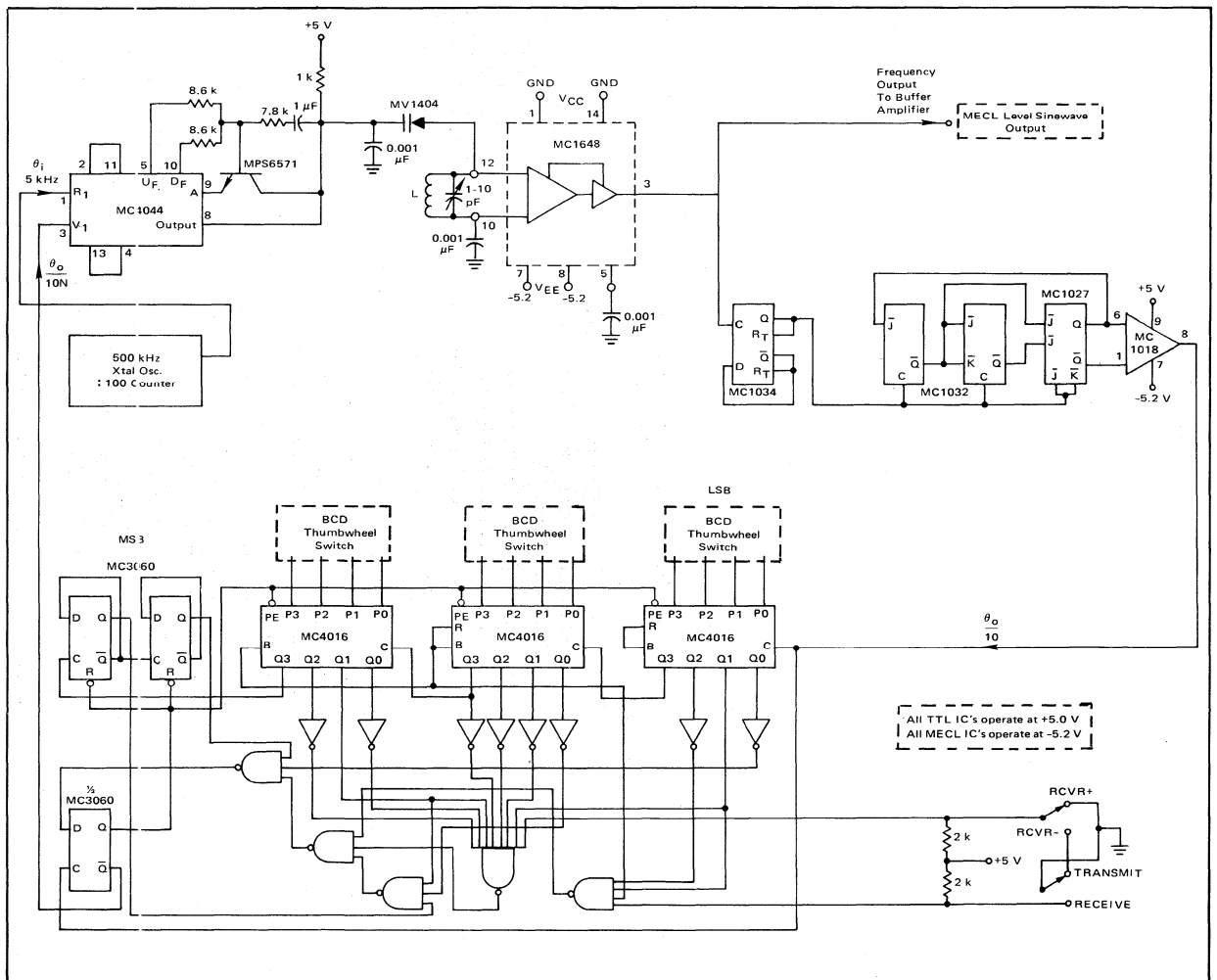

FIGURE 11 – Synthesizer Logic Diagram

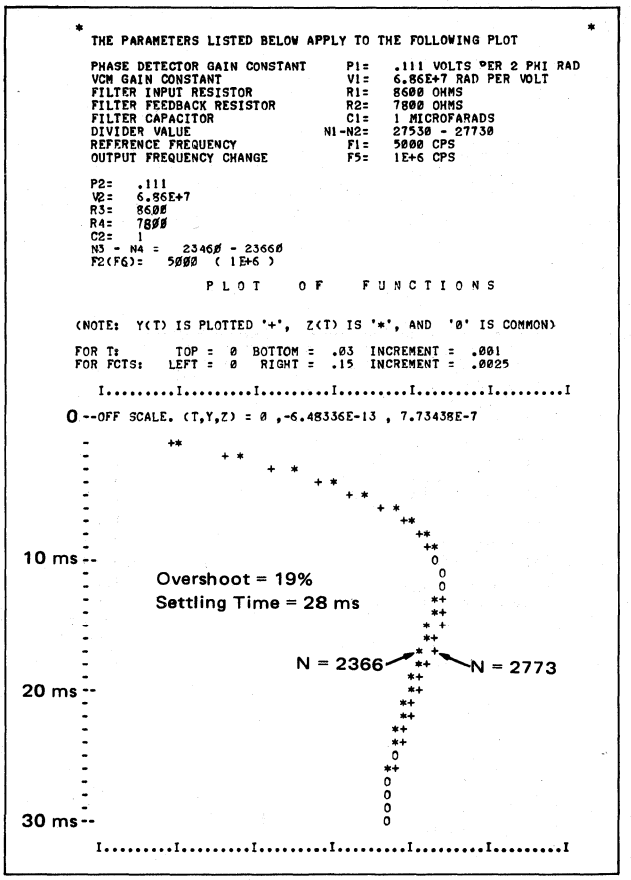

FIGURE 12 – Response Time To 1 MHz Step

REFERENCES

1. Byrne, C. J., "Properties and Design of the Phase-Controlled Oscillator with a Sawtooth Comparator", BSTJ, pp. 559-602, March, 1962.
2. DeLaune, J., "MECL 50 MHz Programmable Counter", Motorola Application Note AN-456.
3. Goldstein, A. J., "Analysis of the Phase-Controlled Loop with a Sawtooth Comparator", BSTJ, Vol. 41, pp. 603-633, March 1962.
4. MECL II MC1000/1200 Series Brochure, Motorola Semiconductor Products Inc., DS 9088, June 1969.
5. MTTL Complex Functions MC4000 Series Brochure, Motorola Semiconductor Products Inc., DS 9108, June 1969.
6. MV1401-5 VVC Data Sheet, Motorola Semiconductor Products Inc., DS 8520 R1, September 1969.
7. MV2201-9 VVC Data Sheet, Motorola Semiconductor Products Inc., DS 8532, May 1969.
8. Schaffner, G., "EPICAP VVC Tuning of Resonant Circuits", Motorola Application Note AN-178A.
9. Thaler, G.J., "Elements of Servomechanism Theory", pp. 33, 1955.
10. Welling, B., "An Integrated Circuit Phase-Locked Loop Digital Frequency Synthesizer", Motorola Application Note AN-438.

AN-535

PHASE-LOCKED LOOP DESIGN FUNDAMENTALS

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INTRODUCTION

The purpose of this application note is to provide the electronic system designer with the necessary tools to design and evaluate Phase Locked Loops (PLL) configured with integrated circuits. The majority of all PLL design problems can be approached using the Laplace transform technique. Therefore, a brief review of Laplace is included to establish a common reference with the reader. Since the scope of this article is practical in nature all theoretical derivations have been omitted hoping to simplify and clarify the content. A bibliography is included for those who desire to pursue the theoretical aspect.

PARAMETER DEFINITION

The Laplace Transform permits the representation of the time response f(t) of a system in the complex domain F(s) This response is twofold in nature in that it contains both the transient and steady state solutions. Thus, all operating conditions are considered and evaluated. The Laplace transform is valid only for positive real time linear parameters; thus, its use must be justified for the PLL which includes both linear and nonlinear functions. This justification is presented in Chapter Three of Phase Lock Techniques by Gardner.[1]

The parameters in Figure 1 are defined and will be used throughout the text.

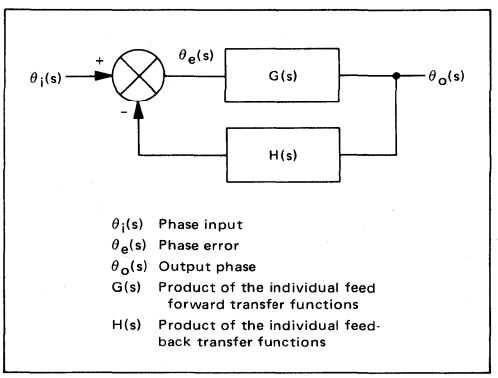

FIGURE 1 – Feedback System

Using servo theory, the following relationships can be obtained.[2]

$$\theta_e(s) = \frac{1}{1 + G(s)\,H(s)}\ \theta_i(s) \qquad (1)$$

$$\theta_o(s) = \frac{G(s)}{1 + G(s)\,H(s)}\ \theta_i(s) \qquad (2)$$

These parameters relate to the functions of a PLL as shown in Figure 2.

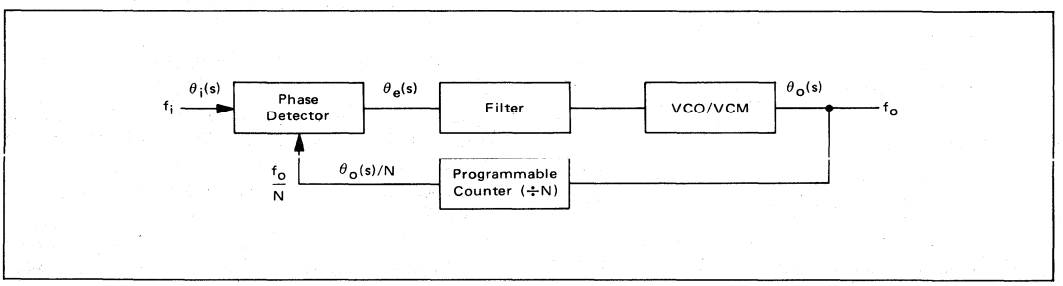

FIGURE 2 – Phase Locked Loop

The phase detector produces a voltage proportional to the phase difference between the signals θ_i and θ_o/N. This voltage upon filtering is used as the control signal for the VCO/VCM (VCM - Voltage Controlled Multivibrator).

Since the VCO/VCM produces a frequency proportional to its input voltage, any time variant signal appearing on the control signal will frequency modulate the VCO/VCM. The output frequency is

$$f_o = N f_i \tag{3}$$

during phase lock. The phase detector, filter, and VCO/VCM compose the feed forward path with the feedback path containing the programmable divider. Removal of the programmable counter produces unity gain in the feedback path (N = 1). As a result, the output frequency is then equal to that of the input.

Various types and orders of loops can be constructed depending upon the configuration of the overall loop transfer function. Identification and examples of these loops are contained in the following two sections.

TYPE – ORDER

These two terms are used somewhat indiscriminately in published literature, and to date there has not been an established standard. However, the most common usage will be identified and used in this article.

The type of a system refers to the number of poles of the loop transfer function G(s) H(s) located at the origin. Example:

$$\text{let} \quad G(s)\,H(s) = \frac{10}{s(s+10)} \tag{4}$$

This is a type one system since there is only one pole at the origin.

The order of a system refers to the highest degree of the polynomial expression

$$1 + G(s)\,H(s) = 0 \triangleq \text{C.E.} \tag{5}$$

which is termed the Characteristic Equation (C.E.). The roots of the characteristic equation become the closed loop poles of the overall transfer function.
Example:

$$G(s)\,H(s) = \frac{10}{s(s+10)} \tag{6}$$

then

$$1 + G(s)\,H(s) = 1 + \frac{10}{s(s+10)} = 0 \tag{7}$$

therefore

$$\text{C.E.} = s(s+10) + 10 \tag{8}$$

$$\text{C.E.} = s^2 + 10s + 10 \tag{9}$$

which is a second order polynomial. Thus, for the given G(s) H(s), we obtain a type 1 second order system.

ERROR CONSTANTS

Various inputs can be applied to a system. Typically these include step position, velocity, and acceleration. The response of type 1, 2, and 3 systems will be examined with the various inputs.

$\theta_e(s)$ represents the phase error that exists in the phase detector between the incoming reference signal $\theta_i(s)$ and the feedback $\theta_o(s)/N$. In evaluating a system, $\theta_e(s)$ must be examined in order to determine if the steady state and transient characteristics are optimum and/or satisfactory. The transient response is a function of loop stability and is covered in the next section. The steady state evaluation can be simplified with the use of the final value theorem associated with Laplace. This theorem permits finding the steady state system error $\theta_e(s)$ resulting from the input $\theta_i(s)$ without transforming back to the time domain.[3]

Simply stated

$$\lim_{t \to \infty} [\theta(t)] = \lim_{s \to o} [s\,\theta_e(s)] \tag{10}$$

Where

$$\theta_e(s) = \frac{1}{1 + G(s)\,H(s)}\ \theta_i(s) \tag{11}$$

The input signal $\theta_i(s)$ is characterized as follows:

$$\text{Step position:} \quad \theta_i(t) = C_p \quad t \geqslant 0 \tag{12}$$

$$\text{Or, in Laplace notation:} \quad \theta_i(s) = \frac{C_p}{s} \tag{13}$$

where C_p is the magnitude of the phase step in radians. This corresponds to shifting the phase of the incoming reference signal by C_p radians:

$$\text{Step velocity:} \quad \theta_i(t) = C_v t \quad t \geqslant 0 \tag{14}$$

$$\text{Or, in Laplace notation:} \quad \theta_i(s) = \frac{C_v}{s^2} \tag{15}$$

where C_v is the magnitude of the rate of change of phase in radians per second. This corresponds to inputing a frequency that is different than the feedback portion of the VCO frequency. Thus, C_v is the frequency difference in radians per second seen at the phase detector.

$$\text{Step acceleration:} \quad \theta_i(t) = C_a t^2 \quad t \geqslant 0 \tag{16}$$

$$\text{Or, in Laplace notation:} \quad \theta_i(s) = \frac{2\,C_a}{s^3} \tag{17}$$

C_a is the magnitude of the frequency rate of change in radians per second per second. This is characterized by a time variant frequency input.

Typical loop G(s) H(s) transfer functions for types 1, 2, and 3 are:

$$\text{Type 1} \quad G(s)\,H(s) = \frac{K}{s(s+a)} \tag{18}$$

$$\text{Type 2}\quad G(s)\,H(s) = \frac{K(s+a)}{s^2} \tag{19}$$

$$\text{Type 3}\quad G(s)\,H(s) = \frac{K(s+a)(s+b)}{s^3} \tag{20}$$

The final value of the phase error for a type 1 system with a step phase input is found by using Equations 11 and 13.

$$\theta_e(s) = \left(\frac{1}{1+\frac{K}{s(s+a)}}\right)\left(\frac{C_p}{s}\right)$$

$$= \frac{(s+a)C_p}{(s^2+as+K)} \tag{21}$$

$$\theta_e(t=\infty) = \lim_{s\to o}\left[s\left(\frac{s+a}{s^2+as+K}\right)C_p\right] = 0 \tag{22}$$

Thus the final value of the phase error is zero when a step position (phase) is applied.

Similarly applying the three inputs into type 1, 2 and 3 systems and utilizing the final value theorem, the following table can be constructed showing the respective steady state phase errors.

TABLE I – Steady State Phase Errors for Various System Types

	Type 1	Type 2	Type 3
Step Position	Zero	Zero	Zero
Step Velocity	Constant	Zero	Zero
Step Acceleration	Continually Increasing	Constant	Zero

A zero phase error identifies phase coherence between the two input signals at the phase detector.

A constant phase error identifies a phase differential between the two input signals at the phase detector. The magnitude of this differential phase error is proportional to the loop gain and the magnitude of the input step.

A continually increasing phase error identifies a time rate change of phase. This is an unlocked condition for the phase loop.

Using Table I the system type can be determined for specific inputs. For instance, if it is desired for a PLL to track a reference frequency (step velocity) with zero phase error, a minimum of type 2 is required.

STABILITY

The root locus technique of determining the position of system poles and zeroes in the s-plane is often used to graphically visualize the system stability. The graph or plot illustrates how the closed loop poles (roots of the characteristic equation) vary with loop gain. For stability all poles must lie in the left half of the s-plane. The relationship of the system poles and zeroes then determine the degree of stability. The root locus contour can be determined by using the following guidelines.[2]

Rule 1 - The root locus begins at the poles of G(s) H(s) (K = 0) and ends at the zeroes of G(s) H(s) (K = ∞). Where K is loop gain.

Rule 2 - The number of root loci branches is equal to the number of poles or number of zeroes, whichever is greater. The number of zeroes at infinity is the difference between the number of finite poles and finite zeroes of G(s) H(s).

Rule 3 - The root locus contour is bounded by asymptotes whose angular position is given by

$$\frac{(2n+1)}{\#P - \#Z}\pi;\ n = 0, 1, 2, \ldots \tag{23}$$

Where #P (#Z) is the number of poles (zeroes).

Rule 4 - The intersection of the asymptotes is positioned at the center of gravity C. G.

$$C.G. = \frac{\Sigma P - \Sigma Z}{\#P - \#Z} \tag{24}$$

Where ΣP (ΣZ) denotes the summation of the poles (zeroes).

Rule 5 - On a given section of the real axis, root loci may be found in the section only if the #P + #Z to the right is odd.

Rule 6 - Breakaway points from negative real axis is given by:

$$\frac{dK}{ds} = 0 \tag{25}$$

Again where K is the loop gain variable factored from the characteristic equation.

Example:

The root locus for a typical loop transfer function is found as follows:

$$G(s)\,H(s) = \frac{K}{s(s+4)} \tag{26}$$

The root locus has two branches (Rule 2) which begin at s = 0 and s = -4 and ends at the two zeroes located at infinity (Rule 1). The asymptotes can be found according to Rule 3. Since there are two poles and no zeroes the equation becomes:

$$\frac{2n+1}{2}\pi = \begin{cases} \frac{\pi}{2} & \text{for } n = 0 \\ \frac{3\pi}{2} & \text{for } n = 1 \end{cases} \tag{27}$$

The position of the intersection according to the Rule 4 is:

$$s = \frac{\Sigma P - \Sigma Z}{\#P - \#Z} = \frac{(-4\ -0) - (0)}{2 - 0}$$

$$s = -2 \qquad (28)$$

The breakaway point as defined by Rule 6 can be found by first writing the characteristic equation.

$$\text{C.E.} = 1 + G(s)\,H(s) = 0$$

$$= 1 + \frac{K}{s(s+4)} = s^2 + 4s + K = 0 \qquad (29)$$

Now solving for K yields

$$K = -s^2 - 4s \qquad (30)$$

Taking the derivative with respect to s and setting it equal to zero then determines the breakaway point.

$$\frac{dK}{ds} = \frac{d}{ds}(-s^2 - 4s) \qquad (31)$$

$$\frac{dK}{ds} = -2s - 4 = 0 \qquad (32)$$

or

$$s = -2 \qquad (33)$$

is the point of departure. Using this information, the root locus can be plotted as in Figure 3.

This second order characteristic equation given by Equation 29 has been normalized to a standard form[2]

$$s^2 + 2\zeta\,\omega_n s + \omega^2_n \qquad (34)$$

where the damping ratio $\zeta = \text{Cos}\,\phi\ (0^o \leqslant \phi \leqslant 90^o)$ and ω_n is the natural frequency as shown in Figure 3.

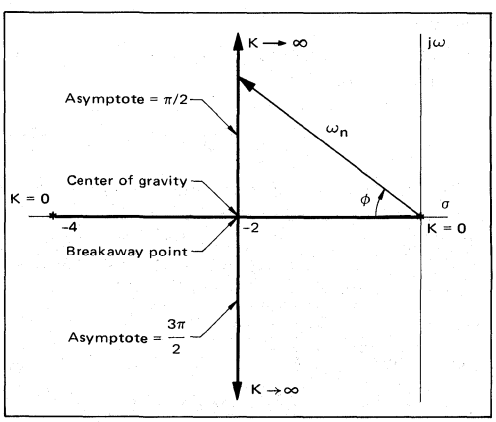

FIGURE 3 – Type 1 Second Order Root Locus Contour

The response of this type 1, second order system to a step input is shown in Figure 4. These curves represent the phase response to a step position (phase) input for various damping ratios. The output frequency response as a function of time to a step velocity (frequency) input is also characterized by the same set of figures.

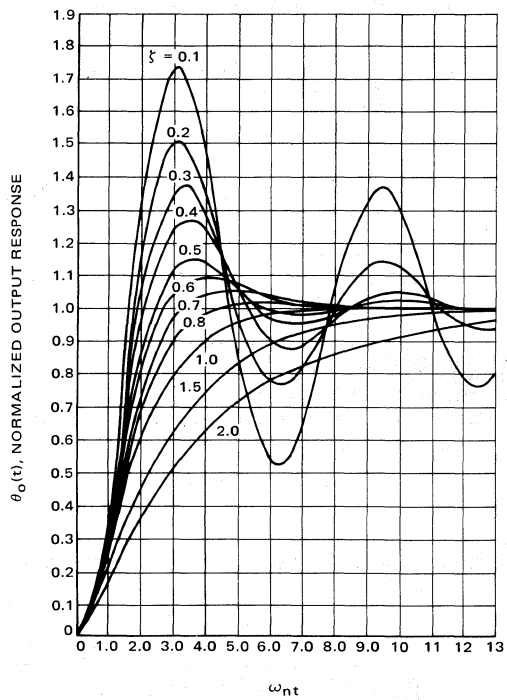

FIGURE 4 – Type 1 Second Order Step Response

The overshoot and stability as a function of the damping ratio ζ is illustrated by the various plots. Each response is plotted as a function of the normalized time $\omega_n t$. For a given ζ and a lock-up time t, the ω_n required to achieve the desired results can be determined. Example:

Assume $\zeta = 0.5$
error $< 10\%$
for $t > 1$ ms

From $\zeta = 0.5$ curve the error is less than 10% of final value for all time greater than $\omega_n t = 4.5$. The required ω_n can then be found by:

$$\omega_n t = 4.5 \qquad (35)$$

or

$$\omega_n = \frac{4.5}{t} = \frac{4.5}{0.001} = 4.5\ \text{k rad/s} \qquad (36)$$

ζ is typically selected between 0.5 and 1 to yield optimum overshoot and noise performance.
Example:

Another common loop transfer function takes the form

$$G(s)\,H(s) = \frac{(s+a)k}{s^2} \qquad (37)$$

This is a type 2 second order system. A zero is added to provide stability. (Without the zero the poles would move along the $j\omega$ axis as a function of gain and the system would at all times be oscillatory in nature.) The root locus shown in Figure 5 has two branches beginning at the origin with one asymptote located at 180 degrees. The center of gravity is s = a; however, with only one asymptote there is no intersection at this point. The root locus lies on a circle centered at s = -a and continues on all portions of the negative real axis to left of the zero. The breakaway point is s = -2a.

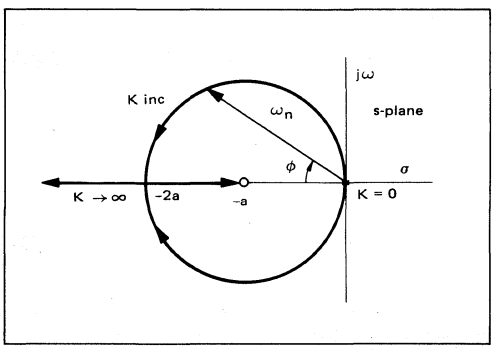

FIGURE 5 – Type 2 Second Order Root Locus Contour

The respective phase or output frequency response of this type 2 second order system to a step position (phase) or velocity (frequency) input is shown in Figure 6. As illustrated in the previous example the required ω_n can be determined by the use of the graph when ζ and the lock up time are given.

BANDWIDTH

The -3 dB bandwidth of the PLL is given by

$$\omega_{-3\ dB} = \omega_n \left(1 - 2\zeta^2 + \sqrt{2 - 4\zeta^2 + 4\zeta^4}\right)^{1/2} \qquad (38)$$

for a type 1 second order[4] system, and by

$$\omega_{-3\ dB} = \omega_n \left(1 + 2\zeta^2 + \sqrt{2 + 4\zeta^2 + 4\zeta^4}\right)^{1/2} \qquad (39)$$

for a type 2 second order[1] system.

PHASE-LOCKED LOOP DESIGN EXAMPLE

The design of a PLL typically involves determining the type of loop required, selecting the proper bandwidth, and establishing the desired stability. A fundamental approach

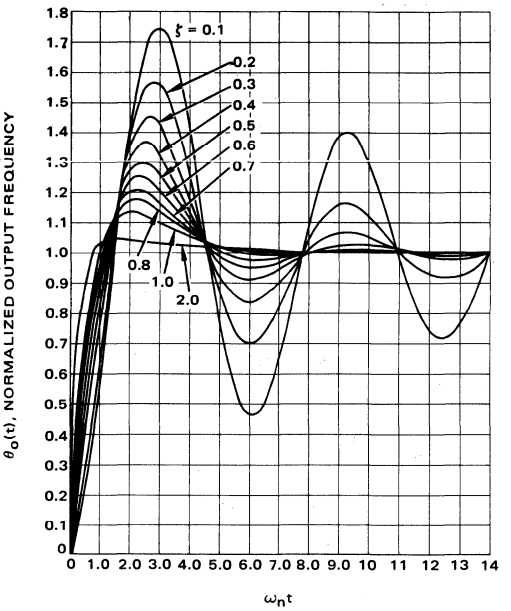

FIGURE 6 – Type 2 Second Order Step Response

to these design constraints is now illustrated. It is desired for the system to have the following specifications:

Output frequency	2.0 MHz to 3.0 MHz
Frequency steps	100 kHz
Phase coherent frequency output	–
Lock-up time between channels	1 ms
Overshoot	< 20%

NOTE: These specifications characterize a system function similar to a variable time base generator or a frequency synthesizer.

From the given specifications the circuit parameters shown in Figure 7 can now be determined.
The devices used to configure the PLL are:

Frequency-Phase Detector	MC4044/4344
Voltage Controlled Multivibrator (VCM)	MC4024/4324
Programmable Counter	MC4016/4316

The forward and feedback transfer functions are given by:

$$G(s) = K_p K_f K_o \qquad H(s) = K_n \qquad (40)$$

where $K_n = 1/N$ (41)

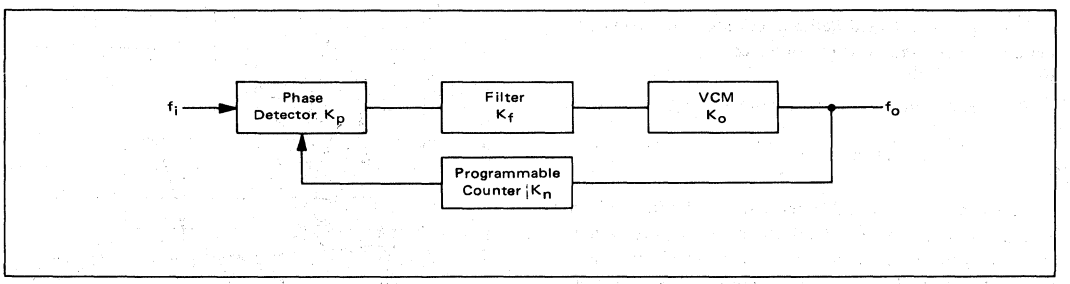

FIGURE 7 – Phase Locked Loop Circuit Parameters

The programmable counter divide ratio K_n can be found from Equation 3.

$$N_{min} = \frac{f_{o\,min}}{f_i} = \frac{f_{o\,min}}{f_{step}} = \frac{2\text{ MHz}}{100\text{ kHz}} = 20 \qquad (42)$$

$$N_{max} = \frac{f_{o\,max}}{f_{step}} = \frac{3\text{ MHz}}{100\text{ kHz}} = 30 \qquad (43)$$

$$K_n = \frac{1}{20} \text{ to } \frac{1}{30} \qquad (44)$$

A type 2 system is required to produce a phase coherent output relative to the input (see Table I). The root locus contour is shown in Figure 5 and the system step response is illustrated by Figure 6.

The operating range of the MC4024/4324 VCM must cover 2 MHz to 3 MHz. Selecting the VCM control capacitor according to the rules contained on the data sheet yields C = 100 pF. The desired operating range is then centered within the total range of the device. The input voltage versus output frequency is shown in Figure 8.

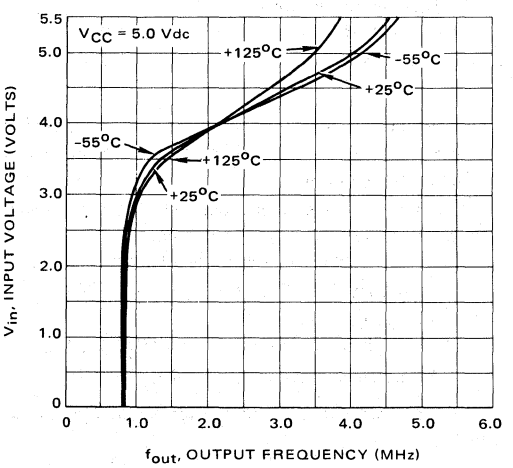

FIGURE 8 – MC4324 Input Voltage versus Output Frequency (100 pF Feedback Capacitor)

The transfer function of the VCM is given by

$$K_O = \frac{K_V}{s} \qquad (45)$$

Where K_V is the sensitivity in radians per second per volt. From the curve in Figure 8, K_V is found by taking the reciprocal of the slope.

$$K_V = \frac{4\text{ MHz} - 1.5\text{ MHz}}{5\text{ V} - 3.6\text{ V}}\ 2\pi \text{ rad/s/V}$$

$$K_V = 11.2 \text{ X } 10^6 \text{ rad/s/V} \qquad (46)$$

Thus

$$K_O = \frac{11.2 \text{ X } 10^6}{s} \text{ rad/s/V} \qquad (47)$$

The s in the denominator converts the frequency characteristics of the VCM to phase, i.e., phase is the integral of frequency.

The gain constant for the MC4044/4344 phase detector is found by [5]

$$K_p = \frac{\text{DF High - UF Low}}{2(2\pi)} = \frac{2.3\text{ V} - 0.9\text{ V}}{4\pi} = 0.111\text{ V/rad} \qquad (48)$$

Since a type 2 system is required (phase coherent output) the loop transfer function must take the form of Equation 19. The parameters thus far determined include K_p, K_O, K_n leaving only K_f as the variable for design. Writing the loop transfer function and relating it to Equation 19

$$G(s)\,H(s) = \frac{K_p\,K_V\,K_n\,K_f}{s} = \frac{K(s+a)}{s^2} \qquad (49)$$

Thus K_f must take the form

$$K_f = \frac{s+a}{s} \qquad (50)$$

in order to provide all the necessary poles and zeroes for

the required G(s) H(s). The circuit shown in Figure 9 yields the desired results.

K_f is expressed by

$$K_f = \frac{R_2Cs + 1}{R_1Cs} \quad \text{for large A} \tag{51}$$

where A is voltage gain of the amplifier.

R_1, R_2, and C are then the variables used to establish the overall loop characteristics.

The MC4044/4344 provides the active circuitry required to configure the filter K_f. An additional low current high β buffering device or FET can be used to boost the input impedance thus minimizing the leakage current from the capacitor C between sample updates. As a result longer sample periods are achievable.

Since the gain of the active filter circuitry in the MC4044/4344 is not infinite, a gain correction factor K_c must be applied to K_f in order to properly characterize the function. K_c is found experimentally to be $K_c = 0.5$.

$$K_{fc} = K_f K_c = 0.5 \left(\frac{R_2Cs + 1}{R_1Cs}\right) \tag{52}$$

(For large gain, Equation 51 applies.)

The PLL circuit diagram is shown in Figure 10 and its Laplace representation in Figure 11.

The loop transfer function is

$$G(s)\,H(s) = K_p K_{fc} K_o K_n \tag{53}$$

$$G(s)\,H(s) = K_p (0.5) \left(\frac{R_2Cs+1}{R_1Cs}\right)\left(\frac{K_v}{s}\right)\left(\frac{1}{N}\right) \tag{54}$$

The characteristic equation takes the form

$$C.E. = 1 + G(s)\,H(s) = 0$$

$$= s^2 + \frac{0.5 K_p K_v R_2}{R_1 N} s + \frac{0.5 K_p K_v}{R_1 CN} \tag{55}$$

Relating Equation 55 to the standard form given by Equation 34

$$s^2 + \frac{0.5 K_p K_v R_2}{R_1 N} s + \frac{0.5 K_p K_v}{R_1 CN}$$

$$= s^2 + 2\zeta\omega_n s + \omega_n^2 \tag{56}$$

Equating like coefficients yields

$$\frac{0.5 K_p K_v}{R_1 CN} = \omega_n^2 \tag{57}$$

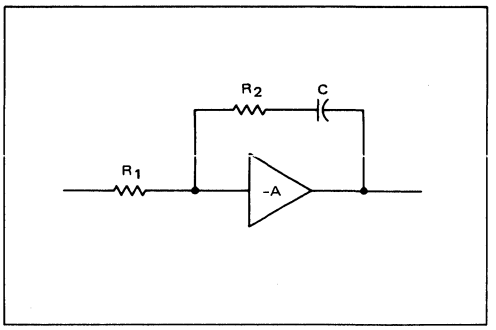

FIGURE 9 – Active Filter Design

and $$\frac{0.5 K_p K_v R_2}{R_1 N} = 2\zeta\omega_n \tag{58}$$

With the use of an active filter whose open loop gain (A) is large ($K_c = 1$), Equations 57 and 58 become

$$\frac{K_p K_v}{R_1 CN} = \omega_n^2 \tag{59}$$

$$\frac{K_p K_v R_2}{R_1 N} = 2\zeta\omega_n \tag{60}$$

The percent overshoot and settling time are now used to determine ω_n. From Figure 6 it is seen that a damping ratio $\zeta = 0.8$ will produce a peak overshoot less than 20% and will settle to within 5% at $\omega_n t = 4.5$. The required lock-up time is 1 ms.

$$\omega_n = \frac{4.5}{t} = \frac{4.5}{0.001} = 4.5 \text{ k rad/s} \tag{61}$$

Rewriting Equation 57

$$R_1 C = \frac{0.5 K_p K_v}{\omega_n^2 N} \tag{62}$$

$$= \frac{(0.5)\,(0.111)\,(11.2 \times 10^6)}{(4500)^2\,(30)}$$

$$R_1 C = 0.00102$$

(Maximum overshoot occurs at N_{max} which is minimum loop gain)

Let $C = 0.5\ \mu F$

Then $$R_1 = \frac{0.00102}{0.5 \times 10^{-6}} = 2.04\ k\Omega$$

Use $R_1 = 2\ k\Omega$

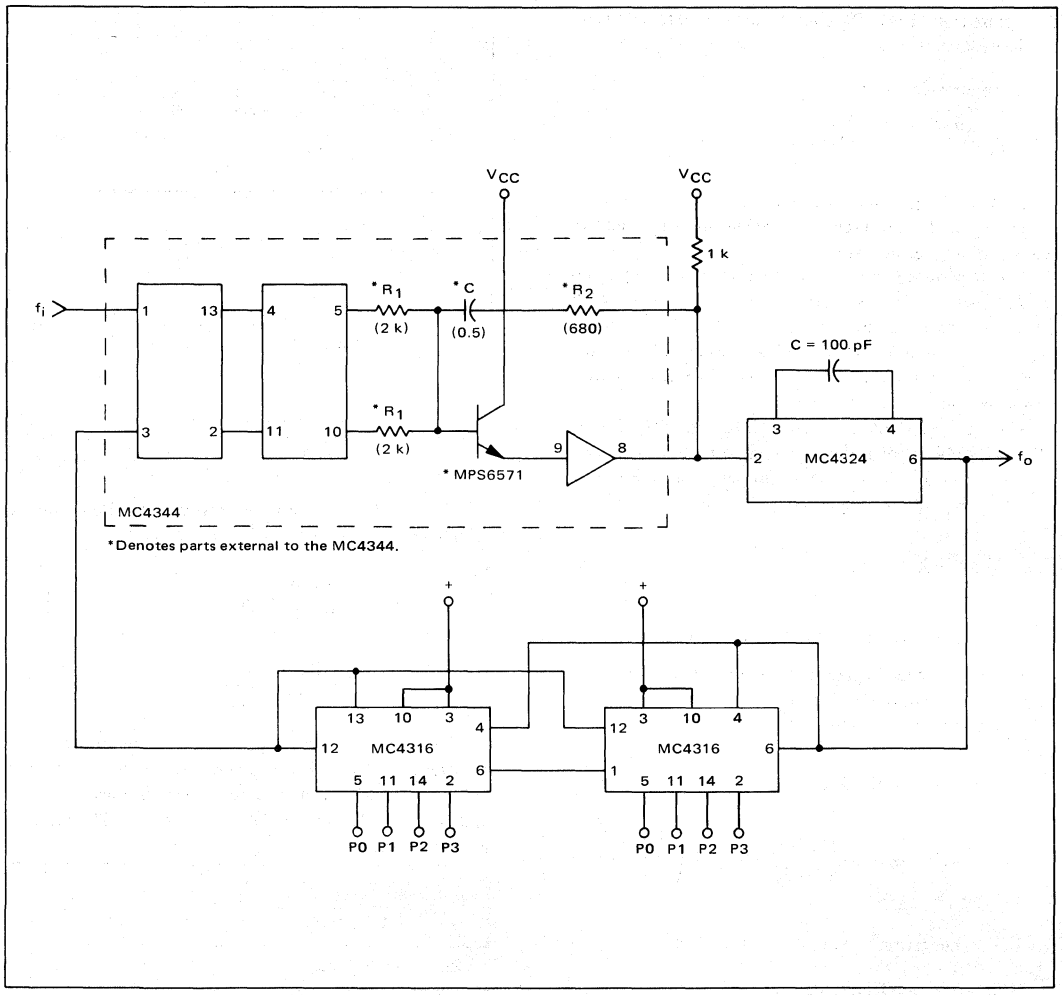

FIGURE 10 – Circuit Diagram of Type 2 Phase Locked Loop

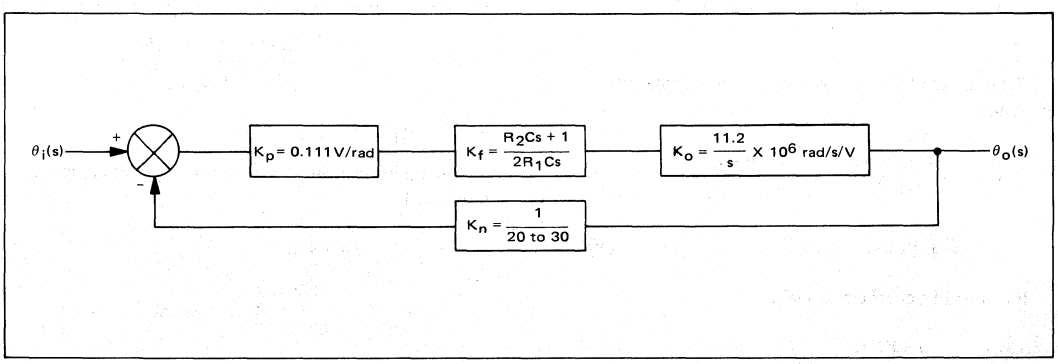

FIGURE 11 – Laplace Representation of Diagram in Figure 10

R_1 is typically selected greater than 1 kΩ.

Solving for R_2 in Equation 58

$$R_2 = \frac{2\zeta\,\omega_n\,R_1 N}{K_p\,K_v(0.5)} = \frac{2\zeta}{C\,\omega_n} \qquad (63)$$

$$= \frac{2(0.8)}{(0.5 \times 10^{-6})(4.5\text{ k})}$$

$$= 711\ \Omega$$

use $R_2 = 680\ \Omega$

All circuit parameters have now been determined and the PLL can be properly configured.

Since the loop gain is a function of the divide ratio K_n, the closed loop poles will vary is position as K_n varies. The root locus shown in Figure 12 illustrates the closed loop pole variation.

The loop was designed for the programmable counter N = 30. The system response for N = 20 exhibits a wider bandwidth and larger damping factor, thus reducing both lock-up time and percent overshoot (see Figure 14).

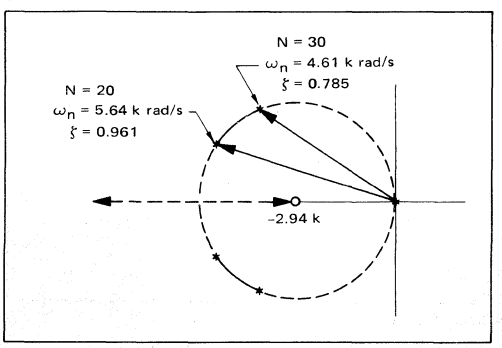

FIGURE 12 – Root Locus Variation

NOTE: The type 2 second order loop was illustrated as a design example because it provides excellent performance for both type 1 and 2 applications. Even in systems that do not require phase coherency a type 2 loop still offers an optimum design.

EXPERIMENTAL RESULTS

Figure 13 shows the theoretical transient frequency response of the previously designed system. The curve N = 30 illustrates the frequency response when the programmable counter is stepped from 29 to 30 thus producing a change in the output frequency from 2.9 MHz to 3.0 MHz. An overshoot of 18% is obtained and the output frequency is within 5 kHz of the final value one millisecond after the applied step. The curve N = 20 illustrates the output frequency change as the programmable counter is stepped from 21 to 20.

Since the output frequency is proportional to the VCM control voltage, the PLL frequency response can be observed with an oscilloscope by monitoring pin 2 of the VCM. The average frequency response as calculated by the Laplace method is found experimentally by smoothing this voltage at pin 2 with a simple RC filter whose time constant is long compared to the phase detector sampling rate but short compared to the PLL response time. With the programmable counter set at 29 the quiescent control voltage at pin 2 is approximately 4.37 volts. Upon changing the counter divide ratio to 30 the control voltage increases to 4.43 volts as shown in Figure 14. A similar transient occurs when stepping the programmable counter from 21 to 20. Figure 14 illustrates that the experimental results obtained from the configured system follows the predicted results shown in Figure 13. Linearity is maintained for phase errors less than 2π, i.e. there is no cycle slippage at the phase detector.

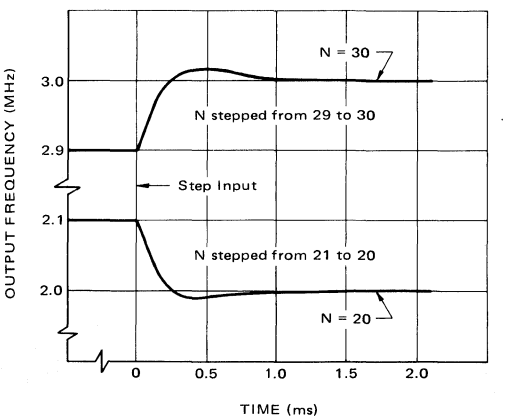

FIGURE 13 – Frequency-Time Response

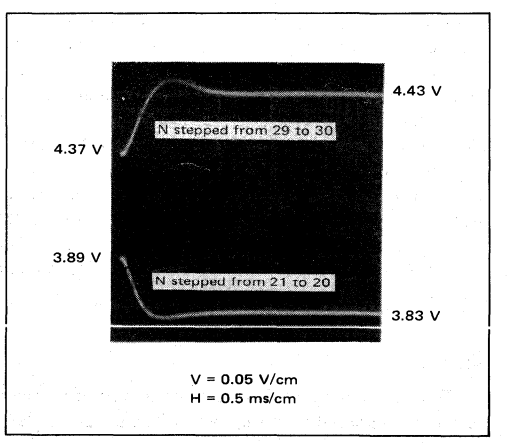

FIGURE 14 – VCM Control Voltage (Frequency) Transient

*THE PARAMETERS LISTED BELOW APPLY TO THE FOLLOWING PLOT

PHASE DETECTOR GAIN CONSTANT	P1 = 0.111 VOLTS PER RADIAN
VCM GAIN CONSTANT	V1 = 1.12 E+7 RAD PER VOLT
FILTER INPUT RESISTOR	R1 = 3900 OHMS ($R1_C$ = 2 k)
FILTER FEEDBACK RESISTOR	R2 = 680 OHMS
FILTER CAPACITOR	C1 = 0.5 MICROFARADS
DIVIDER VALUE	N1-N2 = 29 - 30
REFERENCE FREQUENCY	F1 = 100000 CPS
OUTPUT FREQUENCY CHANGE	F5 = 100000 CPS

P2 = 0.111	C2 = 0.5
V2 = 1.12 E+7	N3 - N4 = 21 - 20
R3 = 3900 ($R1_C$ = 2 k)	F2 (F6) = 100000 (100000)
R4 = 680	

PLOT OF FUNCTIONS

(NOTE: Y(T) IS PLOTTED '+', Z(T) IS '*', AND '0' IS COMMON)

FOR T: TOP = 0 BOTTOM = 0.0015 INCREMENT = 0.00005
FOR FCTS: LEFT = 0 RIGHT = 0.12 INCREMENT = 0.002

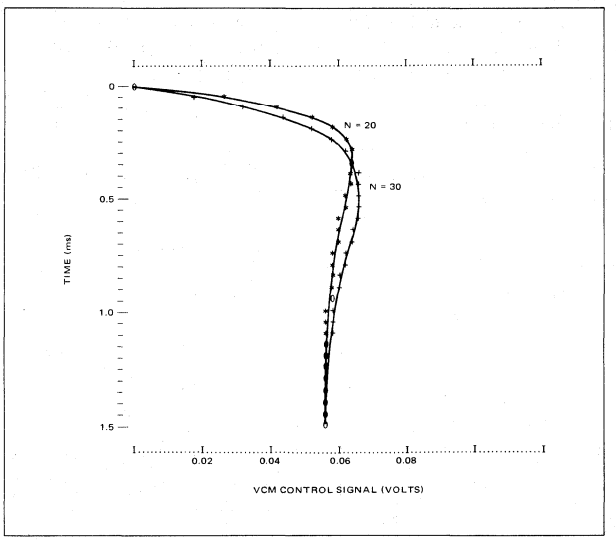

FIGURE 15 – VCM Control Signal Transient

6

Figure 15 is a theoretical plot of the VCM control voltage transient as calculated by a computer program. The computer program is written with the parameters of Equations 58 and 59 (type 2) as the input variables and is valid for all damping ratios of $\zeta \leqslant 1.0$. The program prints or plots the control voltage transient versus time for desired settings of the programmable counter. The lock-up time can then be readily determined as the various parameters are varied. (If stepping from a higher divide ratio to a lower one the transient will be negative.) Figures 14 and 15 also exhibit a close correlation between the experimental and analytical results.

SUMMARY

This application note describes the basic control system techniques required for phase-locked loop design. Criteria for the selection of the optimum type of loop and methods for establishing the desired performance characteristics are presented. A design example is illustrated in a step-by-step approach along with the comparison of the experimental and analytical results.

BIBLIOGRAPHY

1. Topic: Type Two System Analysis
Gardner, F. M., Phase Lock Techniques, Wiley, New York, Second Edition, 1967

2. Topic: Root Locus Techniques
Kuo, B. C., Automatic Control Systems, Prentice-Hall, Inc., New Jersey, 1962

3. Topic: Laplace Techniques
McCollum, P. and Brown, B., Laplace Transform Tables and Theorems, Holt, New York, 1965

4. Topic: Type One System Analysis
Truxal, J.G., Automatic Feedback Control System Synthesis, McGraw-Hill, New York, 1955

5. Topic: Phase Detector Gain Constant
DeLaune, Jon, MTTL and MECL Avionics Digital Frequency Synthesizer, AN532

AN-541

MEDIUM SCALE INTEGRATION IN THE NUMERICAL CONTROL FIELD

Prepared by
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Applications Engineering

INTRODUCTION

A number of integrated circuits of medium scale integration complexity are available for use in the numerical control industry. The majority of these devices use the familiar transistor-transistor logic (TTL) configuration as the basic gating configuration for system design. Figure 1 shows the characteristics of a TTL circuit, a multiple emitter input transistor, followed by a phase splitting transistor and an output circuit whose configuration depends on whether it is a medium- or high-speed circuit. For use in medium scale integration, more commonly known as complex functions, Motorola uses a configuration that employs two forms of TTL gates. Shown in Figure 2 is the low-level gate used within the device itself to drive the internal circuitry not requiring high fanout capabilities. The high-level gate in Figure 3 is used to drive loads on the output pins. The following devices will be discussed in detail, and then their applications to various systems will be presented

MC4016	Decade Programmable Counter
MC4018	Binary Programmable Counter
MC4024	Voltage Controlled Multivibrator
MC4044	Frequency/Phase Detector

MC4016 – DECADE PROGRAMMABLE CASCADEABLE COUNTER

For a single decade counter the clock and gate (G) inputs are normally tied together. When counters are cascaded,

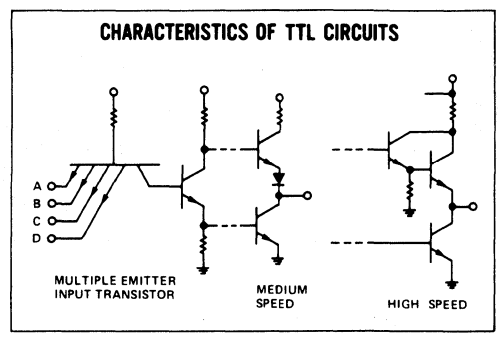


FIGURE 1

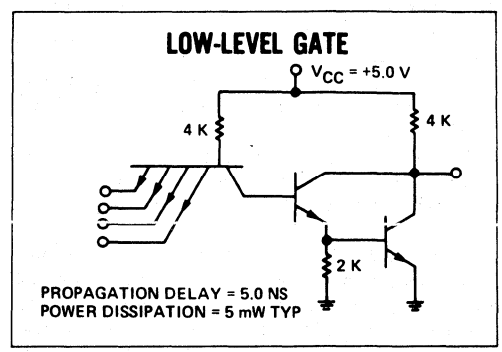


FIGURE 2

all gate inputs are tied to the original input clock. For purposes of explanation we will consider a single decade counter with the clock and gate tied together. The following explanation refers to Figure 4.

The number to be divided by is placed on inputs P1, P2, P4 and P8 in decade form and $\overline{Pn}$ is set high. When $\overline{Pn}$ is momentarily taken low, the reset/preset logic is enabled and the number appearing on the inputs is preset on the outputs Q1, Q2, Q4 and Q8. Once the desired number has been preset, clocking is initiated and the counter counts down from the preset number. When the counter reaches zero (0000) the Buss (B) output goes high and is fed back to the preset circuit. When the feedback is applied to the preset control, the input number is entered back on the outputs of the counter. This causes the Buss output to return to zero. The resultant output is in the form of a

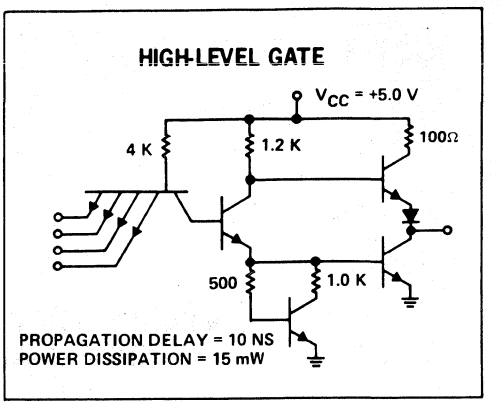


FIGURE 3

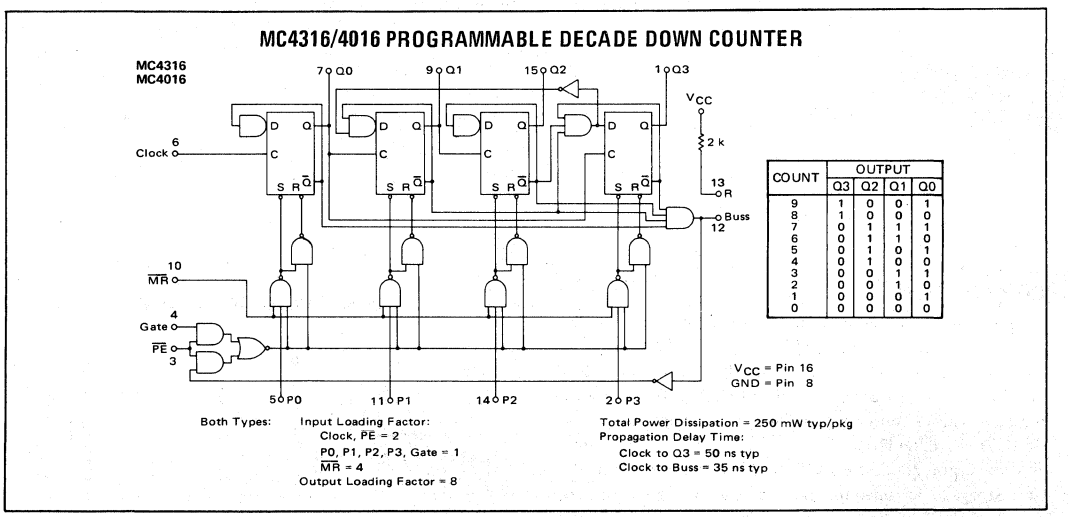
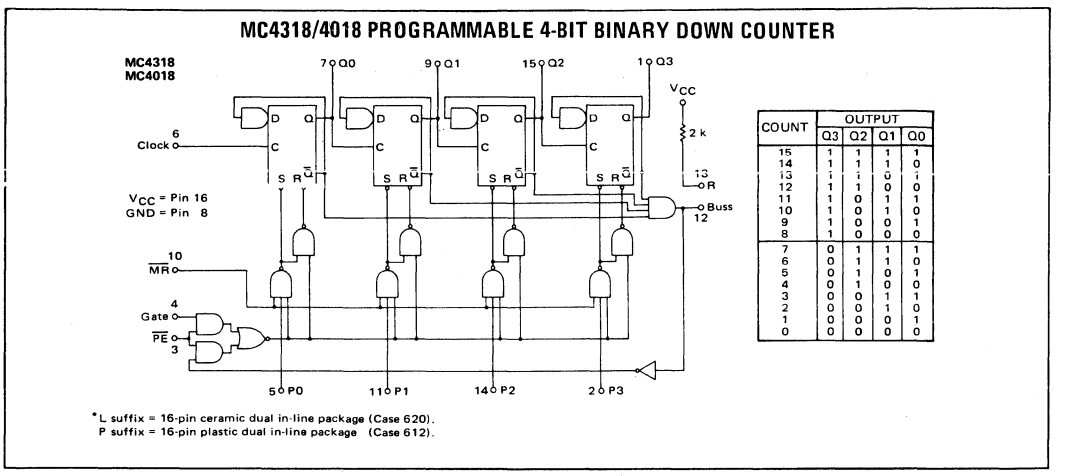


FIGURE 4

pulse. The gate input is to control the pulse width of the Buss output. The Buss output goes to a one when the last clock pulse goes to a one but does not reset the number until the clock goes low. Once the clock goes low both sides of the preset circuit are enabled and the input number can be reset on the outputs of the counter. The pulse from the Buss output is approximately equal to the clock input pulse.

The operation of the decade programmable counter may be further explained by considering an example. Consider the case when it is desired to divide by the number 7 (0111). The number 0111 is placed on inputs P8, P4, P2 and P1 respectively and $\overline{Pn}$ is momentarily taken low. The number 0111 is now on the outputs of the counter. On the first positive transition of the clock the counter goes to 6 (0110). The counter continues to count down on every positive transition of the clock. For the first six clock pulses the Buss output remains low because the count has not reached zero. On the seventh transition the counter goes to 0000 and the Buss output goes high and enables the reset circuit. When the clock goes low the number is again set on the counter outputs and the Buss output goes low. One pulse has now appeared on the Buss output for seven input clock pulses. The counter will continue to divide the clock input by 7 as long as the 7 appears on the inputs. If it is desired to divide by a different number, that number is placed on the appropriate inputs and it will be reset into the counter the next time the counter reaches zero. Since the reset logic is inhibited during normal clocking the new number may be entered while clocking is occurring. If it is desired to enter the new number before the counter reaches zero this can be accomplished by placing the new number on the inputs and taking $\overline{Pn}$ low. The new number will be entered on the outputs and counting will begin from there.



COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

FIGURE 5

Comparisons of MC4016 (Decade Counter – Figure 4) and MC4018 (Binary Counter – Figure 5)

The operation of both programmable counters is approximately the same. The only difference being that the binary counter of Figure 5 is comprised of a divide-by-16 counter with reset/preset logic and the decade counter utilizes a divide-by-10 counter with reset/preset logic. The reset/preset logic for both counters is identical.

The above description applies equally well to both the binary and decade counters with the following two exceptions.

1. The Binary counter will divide-by-16 if the reset logic is inhibited (P1, P2, P4 and P8 high).
2. The Binary counter can be programmed from 0 (0000) to 15 (1111) and the decade counter only from 0 (0000) to 9 (1001). If a larger number than 1001 is programmed into the decade counter the counter will ignore the 8's position and divide by the resulting number. For example, if the programmed number is 14 (1110) the decade counter will divide-by-6 (0110).

Cascading of Counters

Once a thorough understanding of the operation of a single counter has been obtained the cascading of counters is straightforward. The method of cascading is identical for both types of counters. As shown in Figure 6, when cascading counters, the Buss outputs of all packages must be tied together. The same applies to the gate inputs. With all Buss outputs tied together, a one is produced only when all counters hold the zero count. All gate inputs are tied together to insure all counters reset at the same time and to control the width of the output pulse. In addition, one 2-kΩ resistor (R) from one of the packages must be connected to the Buss outputs. This is to provide a pull up resistor for the Buss output gates. The only difference in

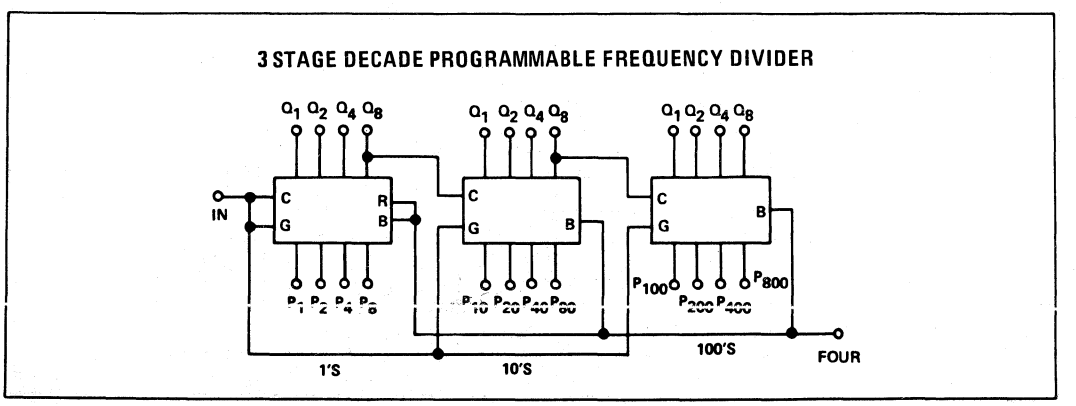


FIGURE 6

the counters being in the method of programming the desired division. The binary counter must be programmed in binary form and the decade in decimal. The reason for the different methods of programming is because of the counting sequence the counters revert to when the reset logic is inhibited. This point will be explained by considering an example for each counter.

Consider the case where decade counters are being used and the desired division is by 325 (0011 0010 0101). The first counter (least significant bit) is programmed to 5 (0101), the second to 2 (0010) and the third (most significant bit) to 3 (0011). After 5 clock pulses the count will be 0000 0010 0011. Since all Buss outputs are ANDed together and 0000 does not exist in the second and third counters, the Buss output remains at zero and the first counter is not reset. The next (sixth) clock pulse produces the count of 1001 0001 0011 or 319. This process continues for 325 pulses until all counters contain 0000. When all counters reach 0000 the Buss outputs go high and the number is reset. One pulse out has been obtained from 325 pulses in. In other words, the clock input has been divided by 325.

For the second case, assume that binary counters are being used and the desired division is again by 325 (0001 0100 0101). The first counter is programmed with 5 (0101), the second to 64 (0100) and the third to 256 (0001). The count proceeds as before for the first five clock pulses. The count is now 0000 0010 1000 reading from least significant to most significant bit. Again the first counter is not reset because all counters do not hold the 0000 count. On the next (sixth) clock pulse the count is 1111 1100 1000 or 319. At this point three things become apparent: 1) the first counter went to a maximum of 1111 instead of 1001 as the decade counters. 2) the outputs are in a straight binary code, and 3) the counters will divide by 16 instead of 10 until they are reset. As before, the Buss output will not go to 1 until there have been 325 clock pulses.

In both cases the results are identical. The only differences occur in the method of coding the input number and the method of counting for the counters.

Because of the difficulty in programming, it is best not to mix types of counters when cascading. An exception to this is when a different counter is used in the most significant position of the cascaded chain. This is true because the most significant counter is always reset when it reaches zero and is never allowed to revert to its natural counting sequence. This feature becomes important in applications where it is desired to divide by numbers in the range of 1000 to 1599. If this is done with all decade counters, four counters would be required. If a binary counter is used in the most significant position only three counters are required (1 binary and 2 decade) without any loss in ease of programming.

MC4324/MC4024 – DUAL VOLTAGE CONTROLLED MULTIVIBRATOR

This circuit consists of two current-mode, emitter-coupled multivibrators, with appropriate level shifting to produce outputs compatible with TTL logic levels. Frequency control is accomplished through the use of voltage-variable current sources that control the voltage charging rate of a single capacitor. The upper operating limit of this VCM is 30 MHz.

Figure 7 shows the schematic of the MC4324/4024. Note that there are multiple B+ and ground connections. This has been done to provide some degree of isolation between units to keep logic current transients out of the oscillator circuit in critical applications. To disable one

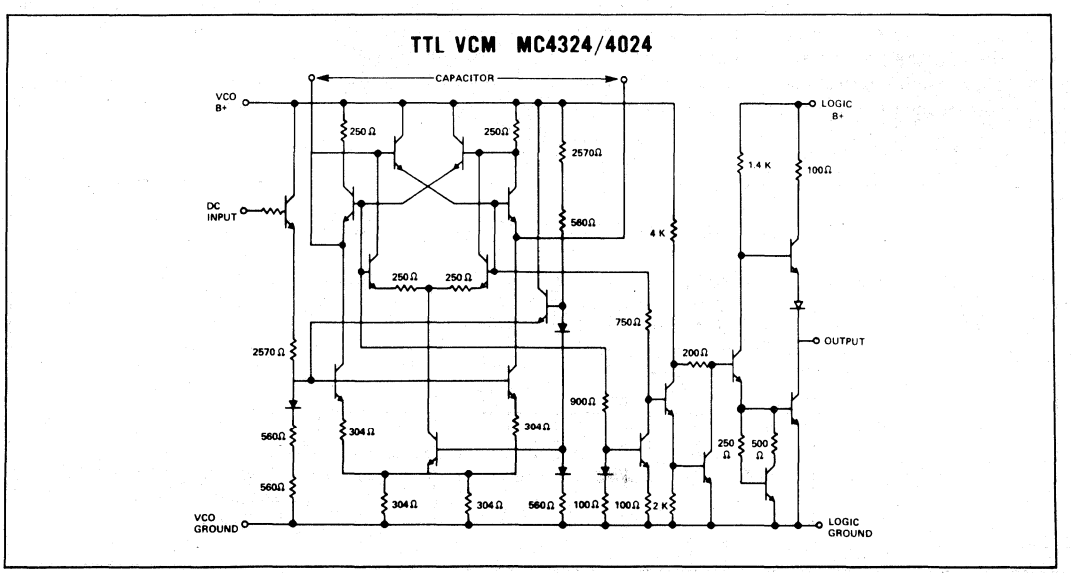


FIGURE 7

VCM, its V_{CC} is disconnected from B+; all grounds must always be connected to insure substrate grounding and good isolation.

The frequency of the voltage controlled oscillator (MC4024) is determined by the external capacitor in the feedback loop. The required value of the capacitor may be determined from either of the following equations.

$$C = \frac{500}{f_{max}} \mu F$$

$$C = \frac{100}{f_{min}} \mu F$$

The frequency of the device is controlled in a nearly linear manner over approximately a 5:1 range by changing the control voltage. The following set of Figures (8 through 13) represent the typical operating characteristics using different values of capacitance in the feedback loop. The curves include room temperature data (25°C) as well as the temperature extremes of -55°C and +125°C.

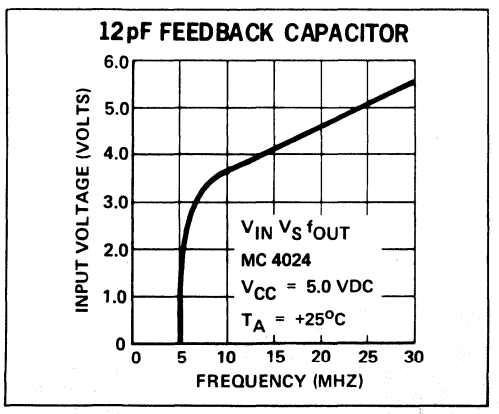


FIGURE 8

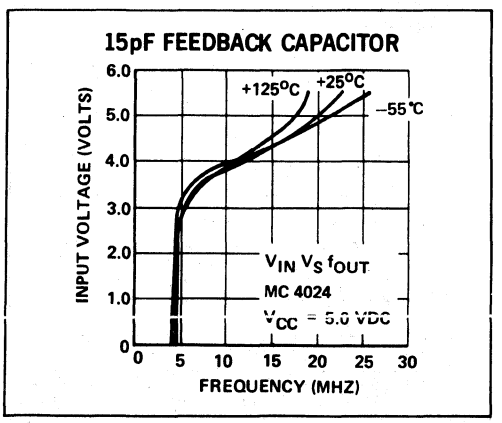


FIGURE 9

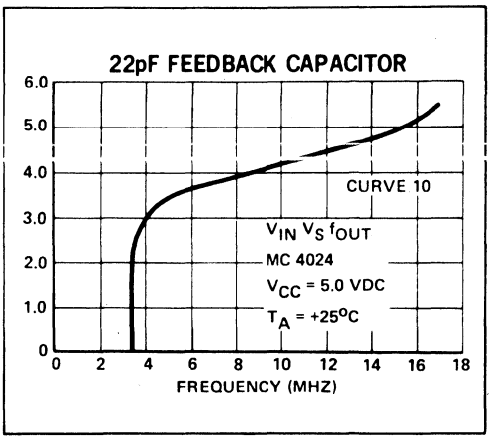


FIGURE 10

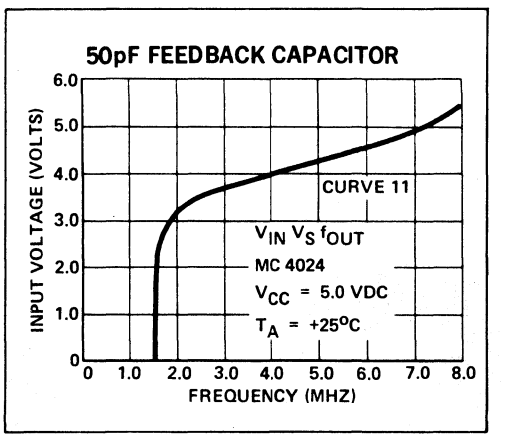


FIGURE 11

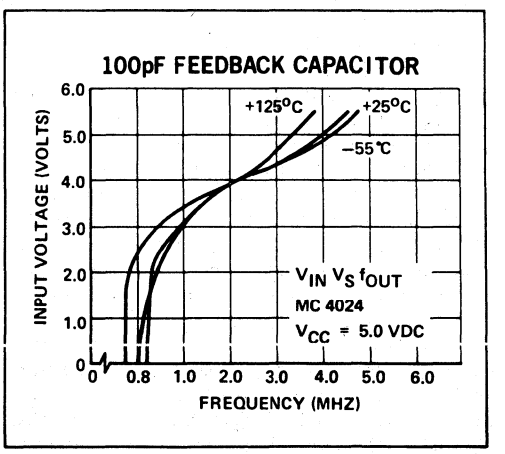


FIGURE 12

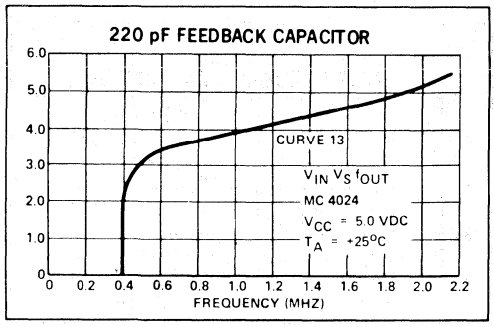


FIGURE 13

Using voltage-variable capacitance diodes in the feedback loop the frequency range of the MC4024 may be increased substantially. The MV1401-03-04-05 hyperabrupt-junction voltage-variable capacitance diodes provide capacitance changes of greater than ten times for a bias change ranging from two-to-ten volts. Figure 14 is the diode capacitance as a function of reverse voltage for these devices.

By using the configuration of Figure 15 the control voltage may be used to bias the voltage variable diodes and change their effective capacitance. The MC1456 is an internally compensated high performance monolithic operational amplifier and is used in the non-inverting feedback mode. Under the conditions shown the gain of the MC1456 is equal to 2. The voltage applied to the MV1403 voltage variable diodes is twice the control voltage V_{in}. Figure 16 relates frequency out, f_o, to voltage in, V_{in}, for Figure 15. Figures 17 and 18 are enlarged portions of Figure 16.

The frequency range of the MC4024 may be decreased by adding resistors from the feedback capacitor terminals to ground. Figure 19 relates frequency out, f_o, to voltage in, V_{in}, using a capacitance of 2000 pF between terminals and two 470 Ω resistors to ground.

MC4344/MC4044 – FREQUENCY/PHASE DETECTOR

Two digital phase detectors and an analog charge pump circuit make up the circuit of Figure 20. The TTL inputs are converted to a dc voltage level for use in frequency discrimination and phase locked loop applications.

The two phase detectors have common inputs. Phase-frequency detector No. 1 is in lock and both outputs are high when the negative transitions of the input (VI) and the reference (RI) are equal in frequency and phase. If VI is lower in frequency or lags in phase, then the U1 output goes low; conversely the D1 output goes low when the VI input is higher in frequency or leads the reference in phase. It is important to note that the duty cycle of the VI input or the RI input is not important since negative transitions control system operation.

Phase detector No. 2 is in lock when the VI input phase lags the reference phase by 90 degrees. In this case, when lock occurs the V2 and D2 outputs go alternately low with equal pulse widths. If the VI input phase lags by more than 90 degrees, U2 will remain low longer than D2. If the VI input phase lags the reference phase by less than 90 degrees,

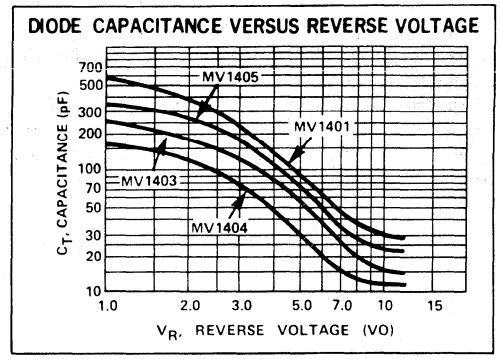


FIGURE 14

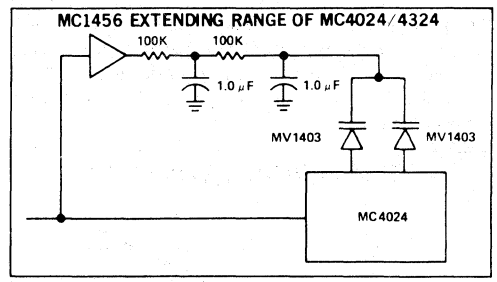


FIGURE 15

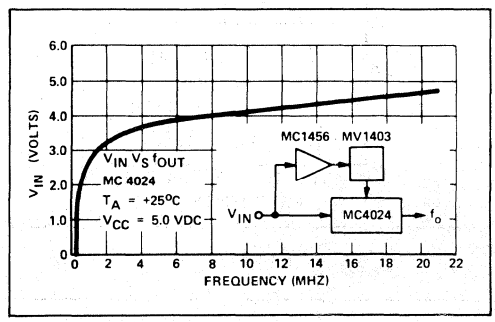


FIGURE 16

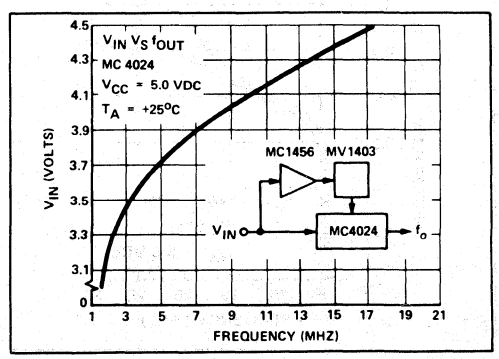


FIGURE 17

D2 remains low longer than U2. In this phase detector the input and the reference must have 50 percent duty cycles.

The charge pump accepts the phase detector outputs and converts them to fixed amplitude positive and negative pulses at the VR and DR outputs respectively. These pulses are applied to a lag-lead active filter which incorporates external capacitors and resistors and the amplifier provided in the circuit. The filter provides a dc voltage proportional to the phase error.

Figure 21 breaks the system down into more detail with a block indicated for the digital section and a block for the analog section. Each section is indicated in more detail in Figures 22 and 23 respectively.

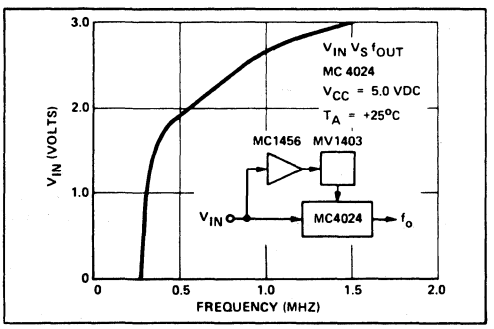


FIGURE 18

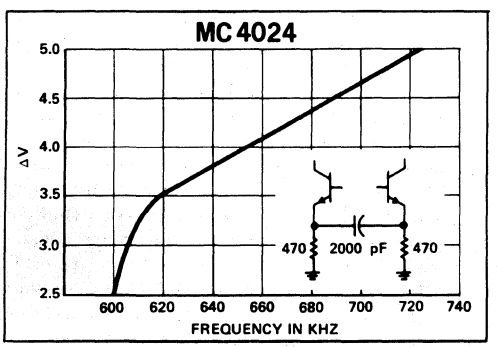


FIGURE 19

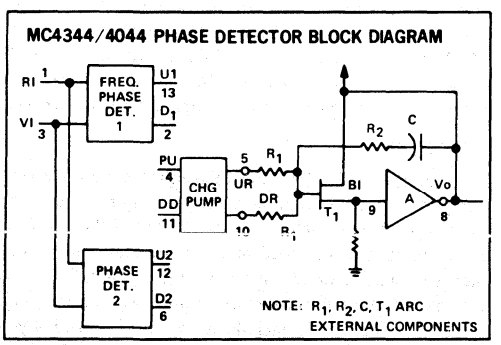


FIGURE 20

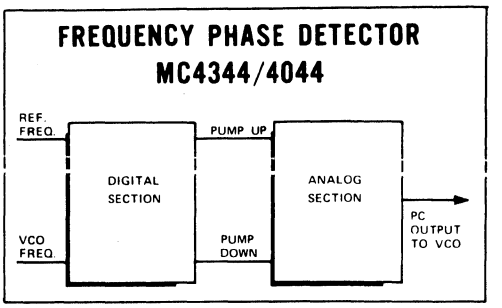


FIGURE 21

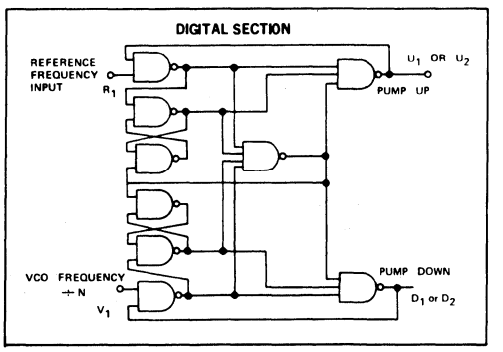


FIGURE 22

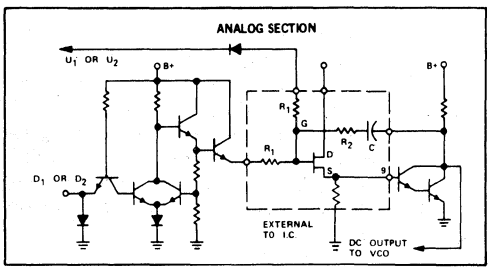


FIGURE 23

APPLICATIONS

Various applications of the previously discussed devices are possible. A number of systems were designed using the MC4024 (Voltage Controlled Multivibrator), the MC4044 (Frequency/Phase Detector) and either the MC4016 (Decade Programmable Down Counter) or the MC4018 (Binary Programmable Down Counter).

Audio Frequency Comparator

A system whereby an unknown frequency is determined by comparing it to a known frequency is shown in Figure 24. The voltage controlled multivibrator, MC4024, is used with a 2 MHz crystal in the feedback loop. Two decade counters (non-programmable) count the frequency down to 20 kHz. Three programmable down counters, MC4016s, provide an output as low in frequency as 20 Hz. One edge

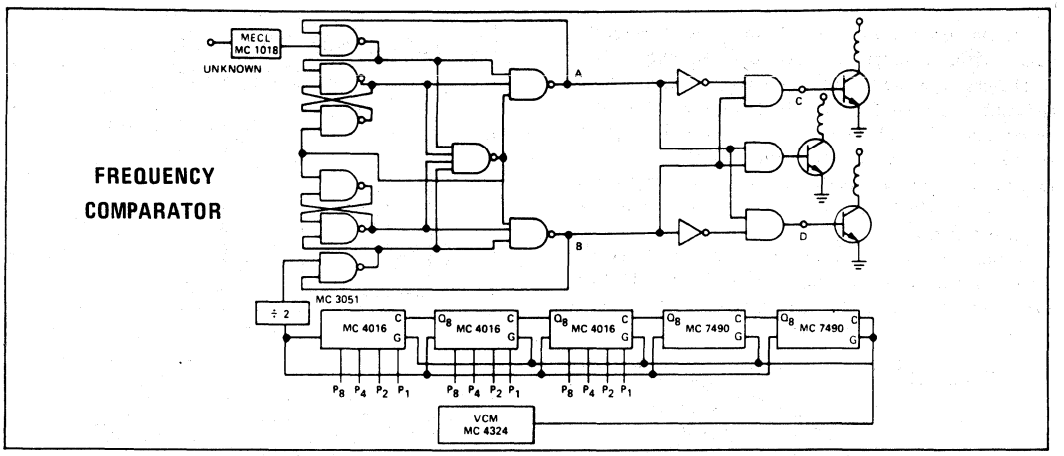


FIGURE 24

trigger flip-flop, MC3051, shapes the output signal of the last programmable counter into a square wave of 50% duty cycle. The unknown signal is fed into a MECL gate, the MC1018 which detects zero crossing of the incoming signal. Using this device the unknown signal may be a sine wave signal and will be converted into a square wave. Both the unknown signal and the reference signal are fed into the digital section of the phase detector. If both signals are the same frequency both points A and B will be at a high level. Outputs C and D will be low and both indicator lights will be off. If the unknown signal is lower in frequency than the reference signal, then point A will go to a low level which in turn will enable the transistor at point C, turning on its indicator light. If the unknown signal is higher in frequency than the reference signal, then point B goes to a low level and the transistor at point D is enabled. The "P" inputs are adjusted for a frequency match–both high indicator and low indicator off – and the unknown frequency determined.

Frequency Synthesizer

The frequency synthesizer loop of Figure 25 achieves a stable state when $F_{VCM} = NF_{ref}$. Until this condition exists, the VCM will continue changing frequency. When the VCM locates the proper frequency the loop locks.

The phase lock loop is used to compare the internally generated frequency of the MC4024 with the external frequency from the reference oscillator and lock the two together. The error voltage that results from comparing the two signals in the digital section of the frequency/phase detector results in a pump-up or pump-down signal to the charge pump, depending on whether the VCM frequency is slower or faster, respectively, than the reference frequency. The charge pump feeds the filter, which determines whether the locking frequency will be underdamped, critically damped, or overdamped. These are a function of the filter elements R1, R2, and C. The filter output feeds the VCM to control its frequency.

Motor Speed Control

Using the previously discussed devices it is possible to provide a motor speed control circuit. Figure 26 is the block diagram of a motor speed control system with the interior phase lock loop shown in more detail in Figure 27. The interior loop accepts the signal from the ac motor pick-up circuit and increases the frequency to the 2 MHz region. The frequency from the interior loop is compared to a reference signal generated from the crystal controlled MC4024 (Voltage Controlled Multivibrator) in conjunction with the MC4018 (Binary Programmable Counter) shown in greater detail in Figure 28. The programmable counter in Figure 28 controls the speed of the ac motor. The ac motor and the entire loop, therefore, respond to the frequency that is programmed on the inputs of the counter. The pick-up circuit of Figure 29 has a phototransistor (MRD310) which picks up a signal from a single strip painted on the shaft of the ac motor. Fiber Optics (not shown on the figure) are used to concentrate the reflection from the shaft and provide the necessary signal to the transistors base. The one-shot multivibrator (MC8601) is necessary to eliminate the effects of shaft jitter which would false trigger the extremely fast response of the MC4044 (Frequency Phase Detector). The ac control circuit which converts the frequency/phase detector output of Figure 28 to a usable signal to control the ac motor is indicated in Figure 30. This circuit utilizes both a bi-lateral switch, and a MAC 2 triac. The conversion of a dc voltage to an ac signal is discussed in more detail in Motorola Application Note AN-482.

CONCLUSION

A number of IC functions of medium scale integrated complexity have been discussed which may be used in the numerical controls field. The application of these devices is not limited to this field but they are usable in various industrial and computer systems. Industrial applications include differential voltmeters, ammeters, counters, etc. Computer applications include system clocks, divide-by-N counters, tape drive controls, etc.

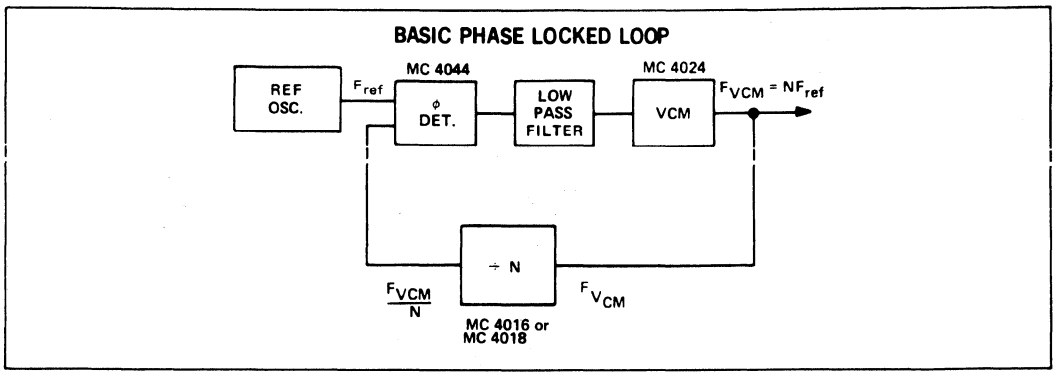


FIGURE 25

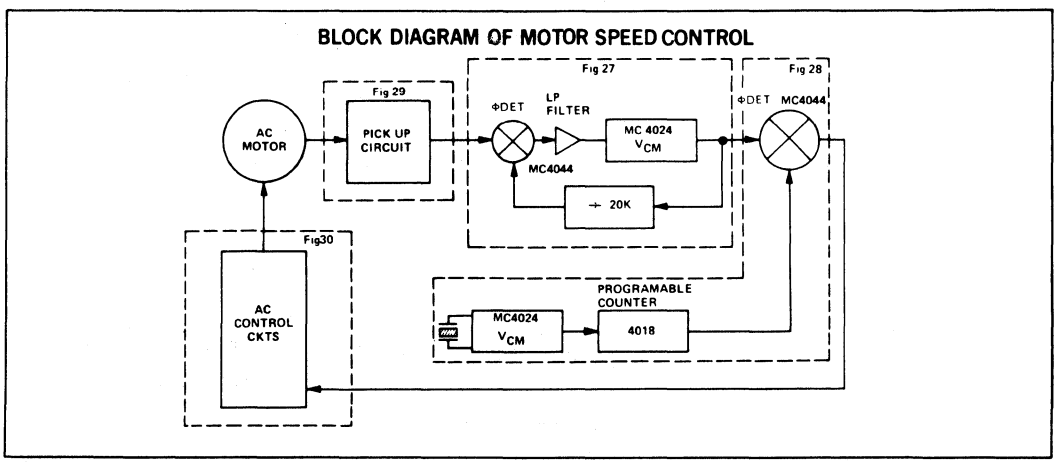


FIGURE 26

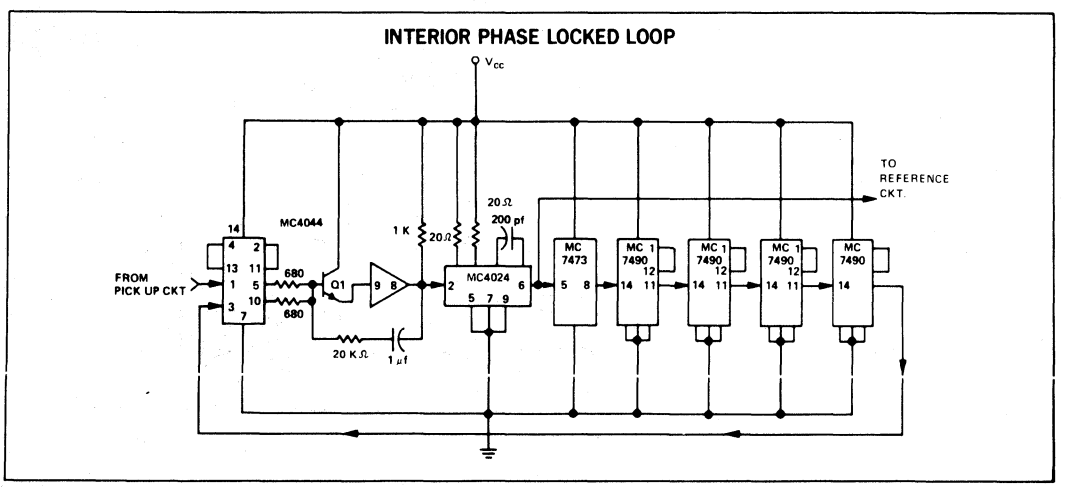


FIGURE 27

FIGURE 28

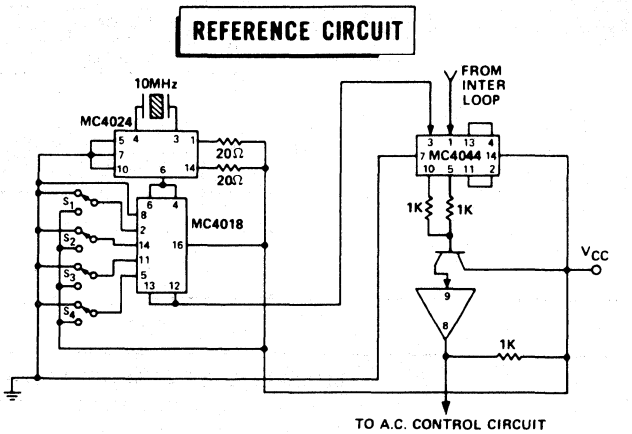


FIGURE 29

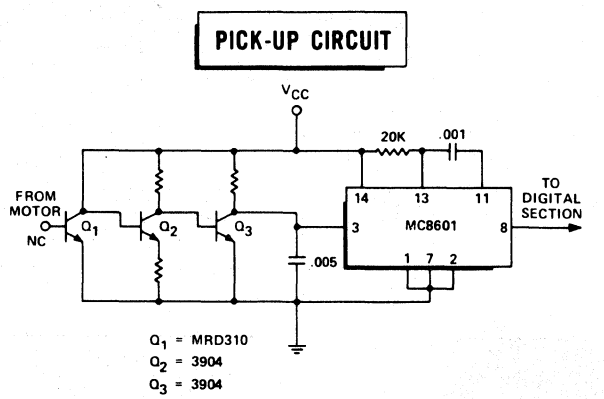
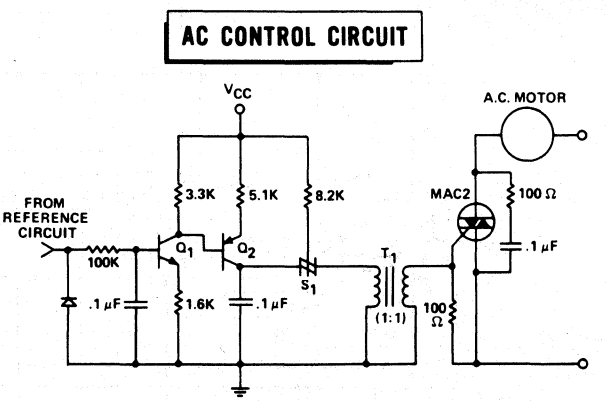


FIGURE 30



AN-553

A NEW GENERATION OF INTEGRATED AVIONIC SYNTHESIZERS

Prepared by

Richard Brubaker
Garth Nash

Applications Engineering

SEVERAL SCHEMES have been previously used to synthesize the required internal mixing frequencies for navigation (NAV), communication (COM), distance measuring equipment (DME), and automatic direction finder (ADF) avionic systems. These have included continuously tuned oscillators, crystal oscillators, and even a few phase locked loops (PLL). The continuously tuned and crystal oscillator designs have matured during the past 10-20 years, however, the phase locked loop technology and its implementation capabilities are still in their infancy.

The phase locked loop principle has been used to a limited degree in electronic design for many years. Some of the first documented applications of the principle date back to the 1930s when they were applied to the synchronous reception of radio signals. The first serious application of the principle appeared in the 1940s when it was applied to synchronization of the vertical and the horizontal sweep generators in television receivers. Since that time, the phase locked loop has been rigorously analyzed and extended to several other applications. Probably some of the most dramatic recent applications have been in the satellite communication systems used for deep space probes. These systems based on the phase locked loop principle have been capable of extracting very low signal amplitudes from high noise environments. Other well-known applications of the principles include coherent transponders, FM discriminators, bit synchronization, signal reconstitution, and the avionic digital frequency synthesizer. The desirability of the phase locked loop for this particular application becomes more obvious from its operating characteristics.

During this past year, several standard product phase locked loop frequency synthesizer integrated circuits began to appear on the market. Prior to this time the loops designed were utilizing discrete, or a mixture of discrete and integrated circuit technology. As a result of advancing IC technology, the capability of establishing standard low cost off-the-shelf phase locked loop monolithic products now presents itself. Presently a complete family of products ranging from VLF through the VHF spectrum is available for various loop configurations.

The approach to utilizing these existing standard products to design a phase locked loop frequency synthesizer is now presented for the NAV, COM, DME, and ADF avionic equipments.

A convenient starting point will be to briefly examine older systems from a historical viewpoint. The object here will be to examine the evolution from one system technique to another and to discuss several major factors involved.

Early versions of the NAV, COM, and ADF systems utilized continuous tuning with the local oscillator and RF front-end tuning capacitors ganged together. One of the disadvantages of this approach was the lack of fast accurate tuning of a desired channel. This need contributed to producing the first crystal controlled system. A bank of crystals was used to generate the desired signal. Since the channels have fixed spacing and can be activated readily through direct switching, the requirement of fast accurate tuning was more readily accomplished. Unfortunately, system complexity was increased because of the large number of crystals required to produce all the possible channels. Even assuming a mixing technique was used, the number of crystals remained significant. The need to reduce the number of crystals leads to the phase locked loop technique of frequency synthesis.

The reduction in the number of crystals in a DME using phase locked loop is also evident. This system typically used to require 20 crystals for 100 channels, whereas now using a phase locked loop, the crystal requirement, system complexity, and cost are reduced.

THE PHASE LOCKED LOOP

The phase locked loop is a closed-loop electronic servo whose output locks onto and tracks an input reference signal. Phase lock is obtained by comparing the phase of the output signal with that of the reference, and any phase difference is converted into an error correction voltage. This error voltage changes the output signal phase to make it track the input.

The servo system has three basic partitions; a phase detector, a loop filter, and a voltage controlled oscillator (VCO), as

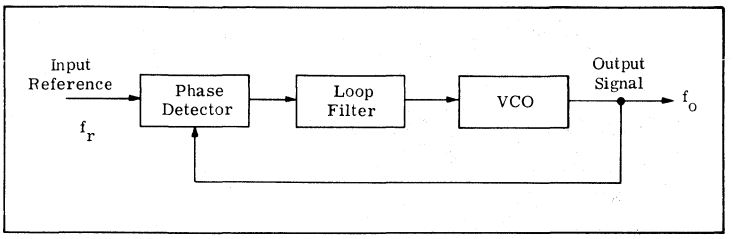
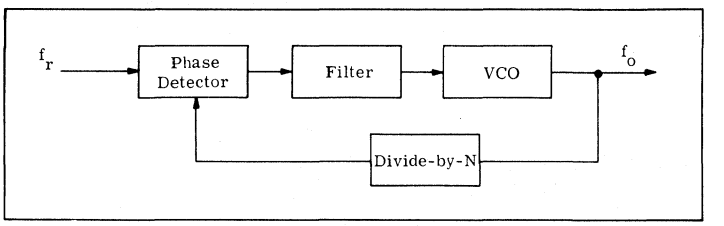


FIGURE 1 – Basic Phase Locked Loop

FIGURE 2 – A Phase Locked Loop with Divide-by-N Feedback



shown in Fig. 1. When the phase difference between the VCO and the input reference signal is constant, the loop is locked. If either the reference or the VCO output changes phase, the phase detector and filter produce a dc error voltage proportional in magnitude and polarity to the signal phase change. This error voltage changes the phase of the VCO by altering its frequency, which locks it onto the reference signal.

When a programmable frequency divider is inserted into the feedback path of the phase locked loop as shown in Fig. 2, the output becomes an integral multiple of the reference frequency. This technique is used for multiple frequency generation in frequency synthesizers. The equation describing the output frequency is

$$f_o = Nf_r \tag{1}$$

The majority of all phase locked loop design problems can be approached using the Laplace transform technique. The Laplace transformation, however, is valid only for positive real time linear parameters; thus its use must be justified for the phase locked loop, which includes both linear and nonlinear functions. For the linear analysis to be correct the following conditions must be met (1)*.

1. The loop time constant must be long compared to the reference period (for example, loop bandwidth is small with respect to the reference frequency).
2. Phase errors are restricted so that cycle slip at the phase detector does not occur.
3. Piecewise linearity over the operational range of all transfer functions is maintained.

The servo parameters are identified in Fig. 3 and will be used throughout the text. Using servo theory, the following relationships can be obtained (2):

$$\theta_e(s) = \frac{1}{1 + G(s)H(s)}\,\theta_r(s) \tag{2}$$

$$\theta_o(s) = \frac{G(s)}{1 + G(s)H(s)}\,\theta_r(s) \tag{3}$$

*Numbers in parentheses designate References at end of paper.

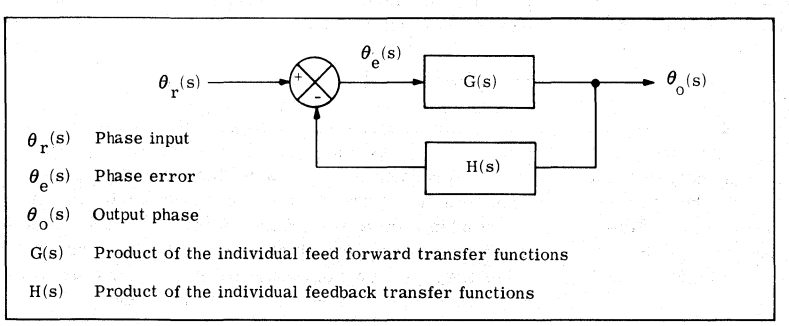


FIGURE 3 – Basic Servo Diagram

These parameters relate to the functions of a phase locked loop as shown in Fig. 4.

The phase detector produces a voltage proportional to the phase difference between the signals θ_r and θ_o/N. This voltage after filtering is used as the control signal for the VCO.

The VCO produces a frequency proportional to its input voltage, and during phase lock the output frequency is N times the reference frequency. The phase detector, filter, and VCO compose the feed forward path while the feedback path contains the divider. Removal of the counter produces unity gain in the feedback path (N = 1). As a result, the output frequency is then equal to the input frequency. Varying N changes the output frequency in increments equal to the reference frequency.

Various types and orders of loops can be constructed depending upon the configuration of the overall loop transfer function. Identification and examples of these loops are contained in the following two sections.

TYPE – ORDER

These two terms are used somewhat indiscriminately in published literature, and to date there has not been an established standard. However, the most common usage will be identified and used in this article.

The type of a system refers to the number of poles of the loop transfer function G(s)H(s) located at the origin of the s-plane. For example let:

$$G(s)H(s) = \frac{10}{s(s+10)} \tag{4}$$

This is a type 1 system since there is only one pole at the origin.

The order of a system refers to the highest degree of the polynomial expression

$$1 + G(s)H(s) = 0 \triangleq \text{C.E.} \tag{5}$$

which is termed the characteristic equation (C.E). The roots of the characteristic equation become the closed loop poles of the overall transfer function. Example:

$$G(s)H(s) = \frac{10}{s(s+10)} \tag{6}$$

then

$$1 + G(s)H(s) = 1 + \frac{10}{s(s+10)} = 0 \tag{7}$$

Therefore,

$$\text{C.E.} = s(s+10) + 10 \tag{8}$$

$$\text{C.E.} = s^2 + 10s + 10 \tag{9}$$

which is a second order polynomial. Thus, for the given G(s)H(s), we obtain a type 1 second order system.

TYPE 1 VERSUS TYPE 2

The first generation of frequency synthesizers utilized what is known as a type 1 design. The type of a servo system is determined by the number of pure integrators (1/s) in the loop. A type 1 loop thus has one integrator in its loop transfer function. Such a design is shown in Fig. 5. The reference signal is derived from a stable frequency source such as a crystal oscillator, and then is divided down to the desired channel spacing. Thus for 10 kHz channel spacing the frequency at point R

FIGURE 4 – Phase Locked Loop Parameters

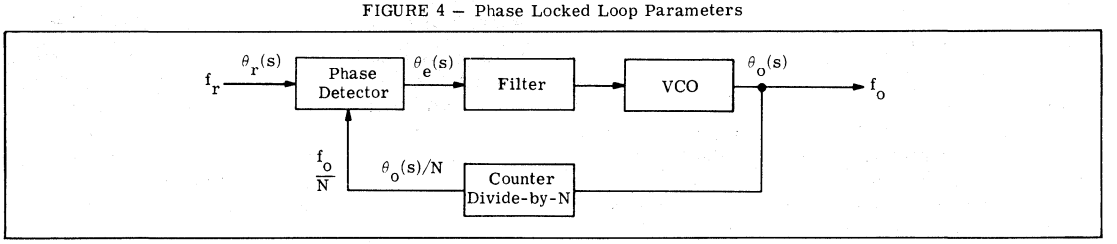
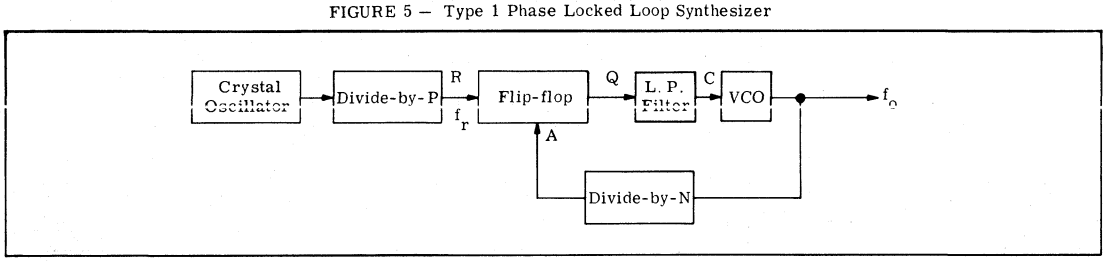


FIGURE 5 – Type 1 Phase Locked Loop Synthesizer



should be 10 kHz. The output frequency, f_o, during phase lock follows the relationship

$$f_o = Nf_r \quad (10)$$

Under steady state conditions there is a constant phase error seen at the flip-flop phase detector. A typical timing waveform is shown in Fig. 6.

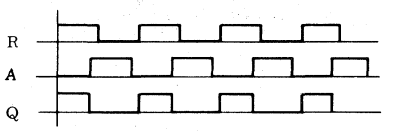


FIGURE 6 – Type 1 Phase Locked Loop Timing Waveform

As the phase of A is moved relative to the reference R, the duty cycle of the flip-flop varies. The control voltage for the VCO is derived by filtering to obtain the average value or dc component of the Q waveform. Therefore, different duty cycles produce different control voltages, thus altering the output frequency. As N varies, the duty cycle automatically adjusts itself until lock is established. Phase lock is said to be established when the phase error at Q is constant.

Any ac component riding on the dc control voltage modulates the VCO. Thus, the spectral purity of the output is a function of the stop band attenuation in the low pass filter. Frequency synthesizers using this technique usually employ a rather sophisticated filter, which yields high attenuation above the cutoff frequency.

Phase detectors that utilize the sample and hold principles are also generally of the type 1 configuration. This approach does not require the degree of filter sophistication, since the control voltage is stored on a holding capacitor rather than being obtained by averaging a time variant waveform. Additional logic is required, however, for producing the properly sequenced timing signals.

Another loop configuration common in frequency synthesis designs is the type 2 loop. A type 2 phase locked loop has two pure integrators ($1/s^2$) in the loop transfer function. This approach is utilized when phase coherency of the received signal is required. The loop maintains a steady state zero phase error for all operating conditions. Avionic equipment requirements usually do not demand phase coherency in the received signal, however, in most cases a type 2 system offers a simpler phase locked loop design. The control voltage for the VCO is derived from the phase detector by integrating the phase error to zero and maintaining that relationship at the phase detector. Steady state error commands are then in the form of delta functions, whose energy is quite small and are, therefore, easily smoothed with a simple filter.

A typical type 2 loop takes the basic form shown in Fig. 7. The phase detector is designed to detect phase errors of either polarity relative to the reference signal and produce the properly polarized error commands necessary to correct the VCO. The low pass filter must include an integrator for storing the proper VCO control voltage during phase lock. The basic transfer characteristics for each of the individual functions are (3):

K_p Phase detector gain constant in volts per radian

K_f Filter transfer functions

$$K_f = \frac{R_2CS + 1}{R_1CS}$$

K_o VCO phase versus voltage characteristic K_V/s

K_V VCO frequency versus voltage sensitivity, radians/sec/V

K_n $1/N$

Note: The s in the denominator of K_o term converts the frequency characteristics of the VCO to phase, for example, phase is the integral of frequency.

STABILITY

The stability criteria of a phase locked loop frequency synthesizer can be approached through the use of root locus techniques. The loop transfer function for a basic type 2 system takes the form

$$G(s)H(s) = \frac{(s + a)K}{s^2} \quad (11)$$

A type 2 system is established by providing the two integrators which appear as the s^2 term in the denominator. This corresponds to two poles located at the origin on the root locus plot. A zero is added to provide stability. (Without the zero the poles would move along the $j\omega$ axis as a function of gain and the closed loop system would be at all times oscillating in nature.) The root locus contour is shown in Fig. 8. A loop gain change of 2:1 will move the poles from $\zeta = 0.707$ to $\zeta = 1.0$.

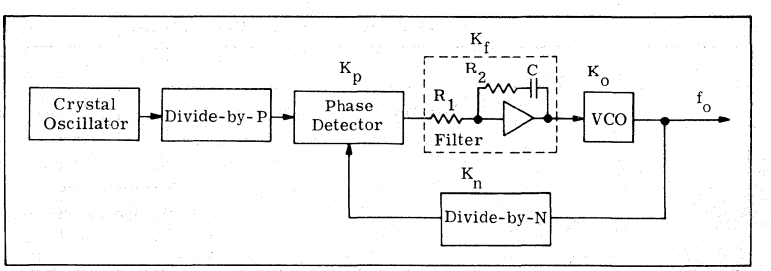


FIGURE 7 – Type 2 Phase Locked Loop

The design of the phase locked loop requires selecting the proper bandwidth and establishing the desired stability. The stability of the loop is best determined by applying a step phase or frequency at the input and determining what the respective output will be. A family of curves, as a function of damping ratio ζ, is shown in Fig. 9. Each response is plotted as a function of the normalized time, $\omega_n t$. For a given ζ and lock-up time, t, the ω_n required to achieve the desired results can be determined. For example, to achieve a lock that is within 10% of its final value after 1 ms with a damping ratio of $\zeta = 0.5$, we see that the $\zeta = 0.5$ curve is within 10% (1:1) at $\omega_n t = 4.5$, or

$$\omega_n = \frac{4.5}{t} = \frac{4.5}{0.001} = 4.5 \text{ k rad/sec} \qquad (12)$$

Using this relationship the natural frequency, ω_n, of the loop has been established.

Another approach to establishing the ω_n is to select the desired $\omega_{-3\text{ dB}}$ of the loop. The -3 dB bandwidth of the phase locked loop is given by

$$\omega_{-3\text{ dB}} = \omega_n \left(1 + 2\zeta^2 + \sqrt{2 + 4\zeta^2 + 4\zeta^4}\right)^{1/2} \qquad (13)$$

for a type 2, second order system. Typical values of the -3 dB bandwidth for various damping ratios are given in Table 1. Thus for a given damping ratio and a desired loop bandwidth the required ω_n can be determined.

For internal loop noise reduction, a relatively wide loop bandwidth is desired so that the loop tracks out or cancels the noise. This technique is used to reduce inherent VCO noise or noise produced during mechanical shock and vibration environments.

The effects of noise external to the loop (phase detector input) are minimized by narrowing the bandwidth. This type of noise is usually minimal in phase locked loop synthesizers, since the frequency standard is derived from a stable crystal oscillator. Frequency modulation of the synthesizer can be accomplished by applying a modulation voltage superimposed upon the control voltage of the VCO. The loop bandwidth must be narrow enough to prevent the loop from responding to the modulation frequency components, thus allowing the VCO to deviate in frequency.

Upon the determination of the desired ω_n, the loop dynamics can now be established. The basic design for a navigation frequency synthesizer is shown as an example. The same approach is utilized for COM, ADF, or DME phase locked loop synthesizers. The system characteristics necessary in the design are given in Table 2.

The VCO operates at the sum of the received frequency and the first IF for high side injection. The programmable counters cannot interface directly with the VCO due to their frequency limitations. Therefore, the VCO output must be translated down to an acceptable frequency. Two methods are

FIGURE 8 — Root Locus Contour

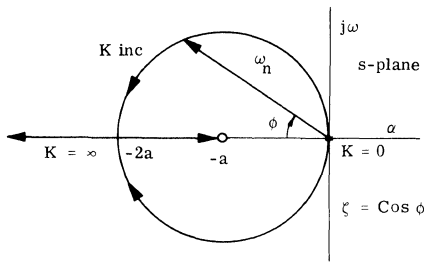


FIGURE 9 — Type 2 Second Order Step Response

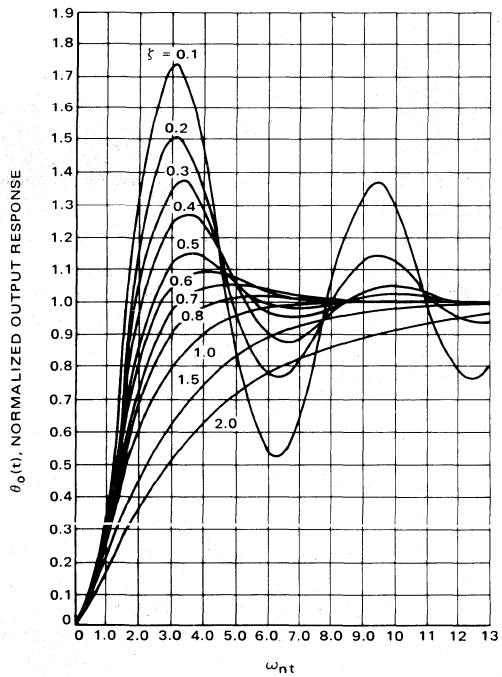


TABLE I

Bandwidth as a Function of Damping Ratio

ζ	$\omega_{-3\text{ dB}}$
0.5	1.82 ω_n
0.7	2.06 ω_n
1.0	2.48 ω_n

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TABLE II

Required Navigation Frequency Synthesizer System Characteristics	
Operating Frequency	108.00 MHz to 118.00 MHz
Channel Spacing	50 kHz
First IF	20 MHz
Lock-up Time	50 milliseconds

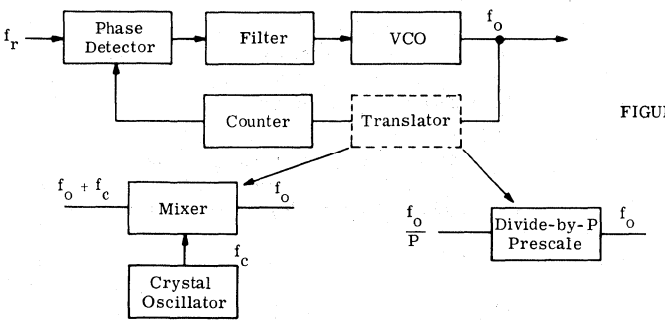


FIGURE 10 — Phase Locked Loop Mixing and Prescaling

available for translating the VHF frequencies down to the operational frequencies of programmable dividers. These are mixing and prescaling as shown in Fig. 10. The mixing technique allows a higher reference frequency, thus a faster lock time (prescaling requires dividing the reference frequency by the prescale division in order to maintain the desired channel spacing). However, as N varies, the loop gain changes altering the bandwidth and stability across the frequency range. Large loop gain variations are usually unacceptable. The mixing technique also requires deriving a local oscillator frequency input, typically from another crystal oscillator, adding another function to the loop.

Prescaling is a less complicated scheme which requires a minimum of packages (typically two-one in the loop and one in the reference chain). The loop becomes more subsystem independent since the number of loop inputs has been reduced. Loop gain variations using this approach have been minimized, thus the loop responds uniformly across the frequency band. Prescaling will be used for this design example.

Using a prescale division of 16, the reference input becomes 3.125 kHz. Selecting an acceptable lock-up curve ($\zeta = 0.8$) from Fig. 9 yields a 5% error within the normalized time, $\omega_n t = 4.5$. This 5% error is relative to the frequency step and not the absolute frequency. The ω_n required to produce this lock time is now found by Eq. 12.

$$\omega_n = \frac{4.5}{t} = \frac{4.5}{0.05} = 90 \text{ rad/sec} \qquad (14)$$

For high side first IF injection, the synthesizer must operate from 128.00-138.00 MHz.

K_n is found by

$$N_{max} = \frac{f_{o\,max}}{f_{ref}} = \frac{1}{K_n} \qquad (15)$$

N_{max} produces the smallest loop gain and, therefore, the smallest bandwidth.

K_p and K_V are calculated by determining the voltage change with phase of the phase detector and the frequency change with voltage of the VCO, respectively. The only parameters remaining to be determined are the R_1, R_2, and C of the filter. These are found by examining the characteristic equation of the loop transfer function.

$$\text{C.E.} = 1 + G(s)H(s) = 0 \qquad (16)$$

$$= 1 + K_p K_f K_o K_n \qquad (17)$$

$$= 1 + K_p\left(\frac{R_2CS + 1}{R_1CS}\right)\left(\frac{K_V}{s}\right)K_n \qquad (18)$$

$$= s^2 + \frac{K_p K_V R_2 K_n}{R_1}s + \frac{K_p K_V K_n}{R_1 C} \qquad (19)$$

This second order characteristic equation has been normalized to a standard form (2)

$$s^2 + 2\zeta\omega_n s + \omega_n^2 \tag{20}$$

Equating like coefficients yields

$$2\zeta\omega_n = \frac{K_p K_V R_2 K_n}{R_1} \tag{21}$$

$$\omega_n^2 = \frac{K_p K_V K_n}{R_1 C} \tag{22}$$

Solving for R_1C in Eq. 22 gives

$$R_1C = \frac{K_p K_V K_n}{\omega_n^2} \tag{23}$$

The time constant R_1C is set by selecting the appropriate pair of values. Theoretically the value of each component is not important as long as their product is properly maintained. The practical aspect of component selection then becomes the basis.

R_2 is found by substituting Eq. 22 into Eq. 21 yielding

$$R_2 = \frac{2\zeta}{\omega_n C} \tag{24}$$

All circuit parameters have now been determined and the phase locked loop can be properly constructed.

Several practical aspects are involved in constructing such a synthesizer. For instance, the loop is very sensitive to noise at the filter and VCO. As identified earlier any ac component on the control voltage will result in frequency modulation at the VCO output. Consequently, the power lines must be decoupled for acceptable spectral purity. Additional RC decoupling and roll off can be placed between the filter output and the VCO control voltage input. The time constant of this additional circuitry should be long compared to the reference period, but short relative to the loop lock time. By using these ground rules, additional filtering of the reference sidebands is obtained without modifying the loop response or bandwidth.

An important feature of such a phase locked loop design is the absence of potentiometers, and variable inductors or capacitors. There are no adjustments to be performed during production testing nor are there any components that require periodic calibration.

A frequency synthesizer covering the NAV/COM band was designed and built utilizing the standard products identified in Fig. 11. The lock-up time was selected arbitrarily to be 50 ms, thus producing a -3 dB loop bandwidth of 14 Hz. A photograph of the output spectrum of the finished circuit is shown in Fig. 12. This is contrasted to Fig. 13, which illustrates a crystal oscillator operating in the same frequency range. Fig. 14 displays the synthesizer spectral output over a wider frequency range than Fig. 12, thus identifying adjacent channel levels.

SYSTEM FLEXIBILITY

Digital synthesizers also have the capability of being programmed externally through the use of computer techniques. Frequency selection of each avionic system can be easily controlled from a central command station. Thus, programming a computer prior to takeoff would provide all the desired frequencies for stations along the flight path. In-flight selection of a particular address properly programs all the various equipments. This concept relieves the pilot of work load, especially in crowded airway environments.

Fig. 15 identifies the basic functions required to design a complete centrally controlled equipment package. Station frequencies that are to be utilized are programmed into a memory by the keyboard. The complete flight plan is stored in

FIGURE 11 – NAV/COM Frequency Synthesizer

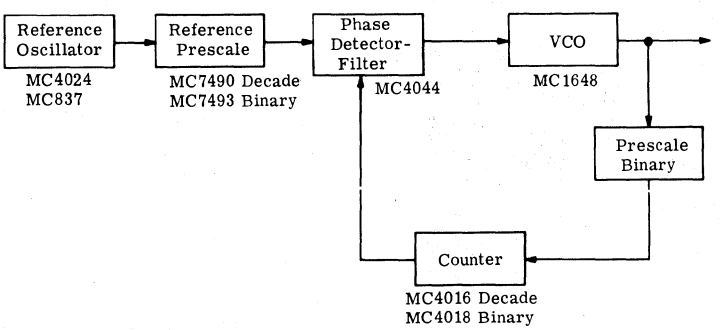
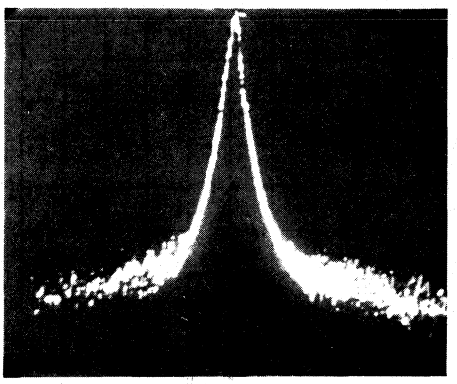


FIGURE 12 – Phase Locked Loop Spectrum



Scan Width	2 kHz/Div
Bandwidth	0.3 kHz
Video Filter	100 Hz
Tuning Stab	On
Scan Time	0.1 Sec/Div
Log Scale	

FIGURE 13 – Crystal Oscillator Spectrum

Scan Width	2 kHz/Div
Bandwidth	0.3 kHz
Video Filter	100 Hz
Tuning Stab	On
Scan Time	0.1 Sec/Div
Log Scale	

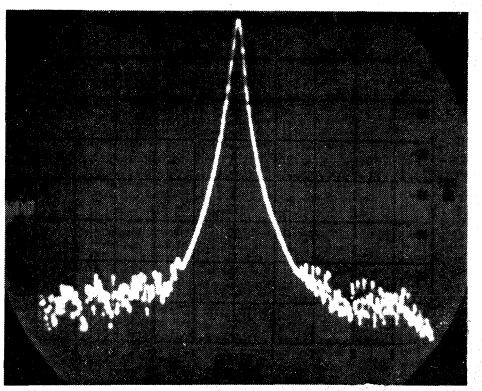


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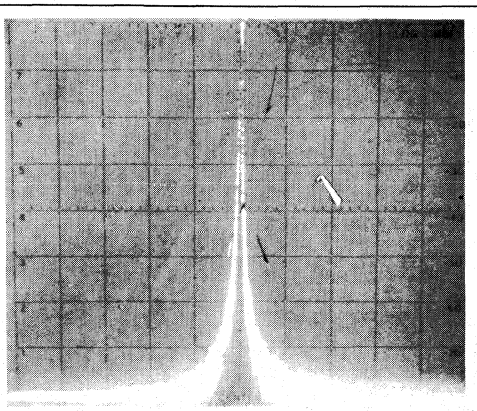
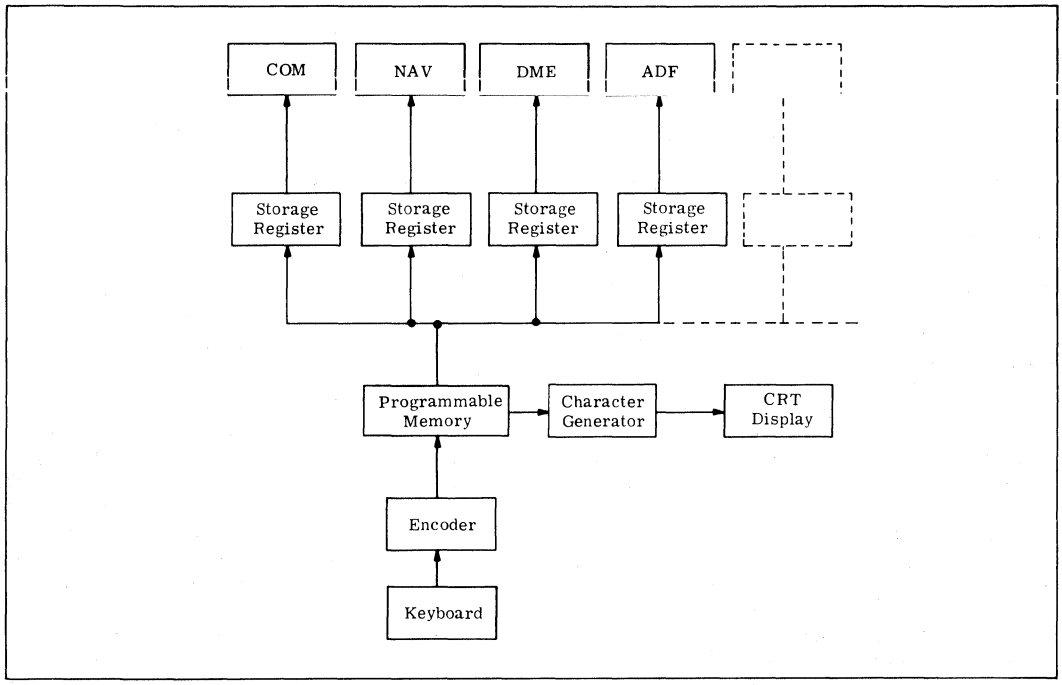
FIGURE 14 – Phase Locked Loop Spectrum



Scan Width	50 kHz/Div
Bandwidth	1 kHz
Video Filter	100 Hz
Tuning Stab	On
Scan Time	0.5 sec/cm
Log Scale	

FIGURE 15 – Central Command Station



conjunction with possible station alternates. Individual system control is maintained by simply reprogramming the data contained in a particular address.

The present trends of semiconductor technology are now making a system of this type feasible using standard product. devices. These standard products take the form of keyboard encoders, character generators, programmable and read-only memories, and lengthy shift registers. Collectively these functions give a new dimension to avionic system design.

REFERENCES

1. F. M. Gardner, "Phase Lock Techniques." Second ed. New York: Wiley, 1967.

2. B. C. Kuo, "Automatic Control Systems." New Jersey: Prentice-Hall, Inc., 1962.

3. Garth Nash, "Phase Locked Loop Design Fundamentals." Motorola Semiconductor Products, Inc., Application Note AN-535.

AN-564

AN ADF FREQUENCY SYNTHESIZER UTILIZING PHASE-LOCK-LOOP I/Cs

Prepared by
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Applications Engineering

INTRODUCTION

This report describes an IC phase-lock loop frequency synthesizer suitable for the local oscillator function in aircraft ADF equipment. An ADF oscillator must provide continuous 1 kHz channel spacing over the required frequency range. The required range of ADF equipment is 200 kHz to 1699 kHz – usually in three bands. The three bands are 200 kHz to 399 kHz, 400 kHz to 829 kHz and 830 kHz to 1699 kHz.

The synthesizer described in this report is intended for frequency conversion to an IF frequency of 10.7 MHz. That is, when the synthesizer is programmed to 200 kHz the actual output frequency is 10.7 MHz higher or 10.9 MHz. Since the actual frequency range is relatively small (10.9 MHz to 12.399 MHz), a simple low-pass filter provides filtering over one band rather than the usual three, i.e., one filter covers the whole band for channels between 200 kHz and 1699 kHz. If a lower IF frequency such as 455 kHz is required, an additional mixer can be used to down-convert to 455 kHz. Another report will be available in the near future describing an ADF frequency synthesizer for 455 kHz IF applications.

A basic circuit description, performance data and circuit schematic is provided. In addition, an actual printed circuit board layout is provided.

CIRCUIT CONSIDERATIONS

The frequency synthesizer described in this report utilizes a digital phase-lock loop (see Figure 1). This loop is implemented with standard off-the-shelf ICs especially designed by Motorola for digital frequency synthesizer applications (see Figure 2). Several discrete transistors are used as translators and amplifiers for convenience and improved loop performance.

CIRCUIT DESCRIPTION

The 100 kHz reference crystal oscillator* (MC837P, see Figure 3) is followed by two decade counters (MC7490P), a dual J-K flip-flop wired as a divide-by-4 (MC7479P) and a one-shot multivibrator (MC8601P) – see Figure 4. The resultant pulse train has a 250 Hz repetition rate with approximately a 200 μs pulse width. The divide-by-4 function compensates for the divide-by-4 pre-scaler (so the programming switches read correctly.) Consequently, even though the input reference signal to the phase detector (MC4044P) is at a frequency of 250 Hz, the actual channel spacing is 1 kHz. The one-shot multivibrator reduces the

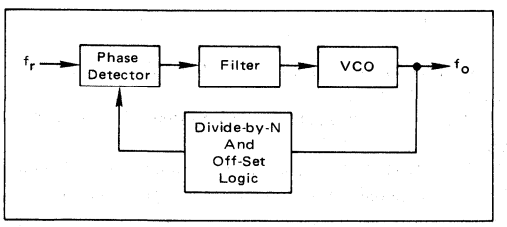


FIGURE 1 – A Phase Locked Loop with Divide-by-N Feedback

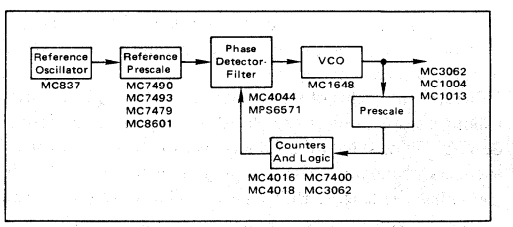


FIGURE 2 – Phase Lock Loop Frequency Synthesizer Using Motorola ICs

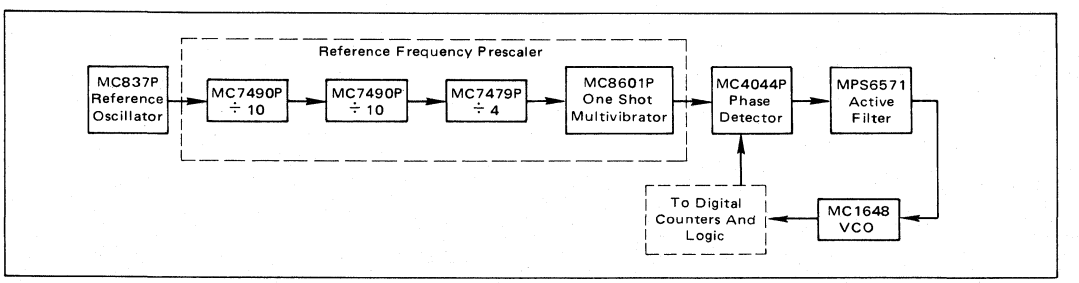


FIGURE 3 – Block Diagram of Oscillator, Reference Frequency Prescaler, Phase Detector, Filter and VCO

*The crystal oscillator shown provides a convenient reference source if a standard T^2L oscillator is not available. This does not imply, however, that it is an adequate or recommended replacement for a T^2L oscillator (commercial).

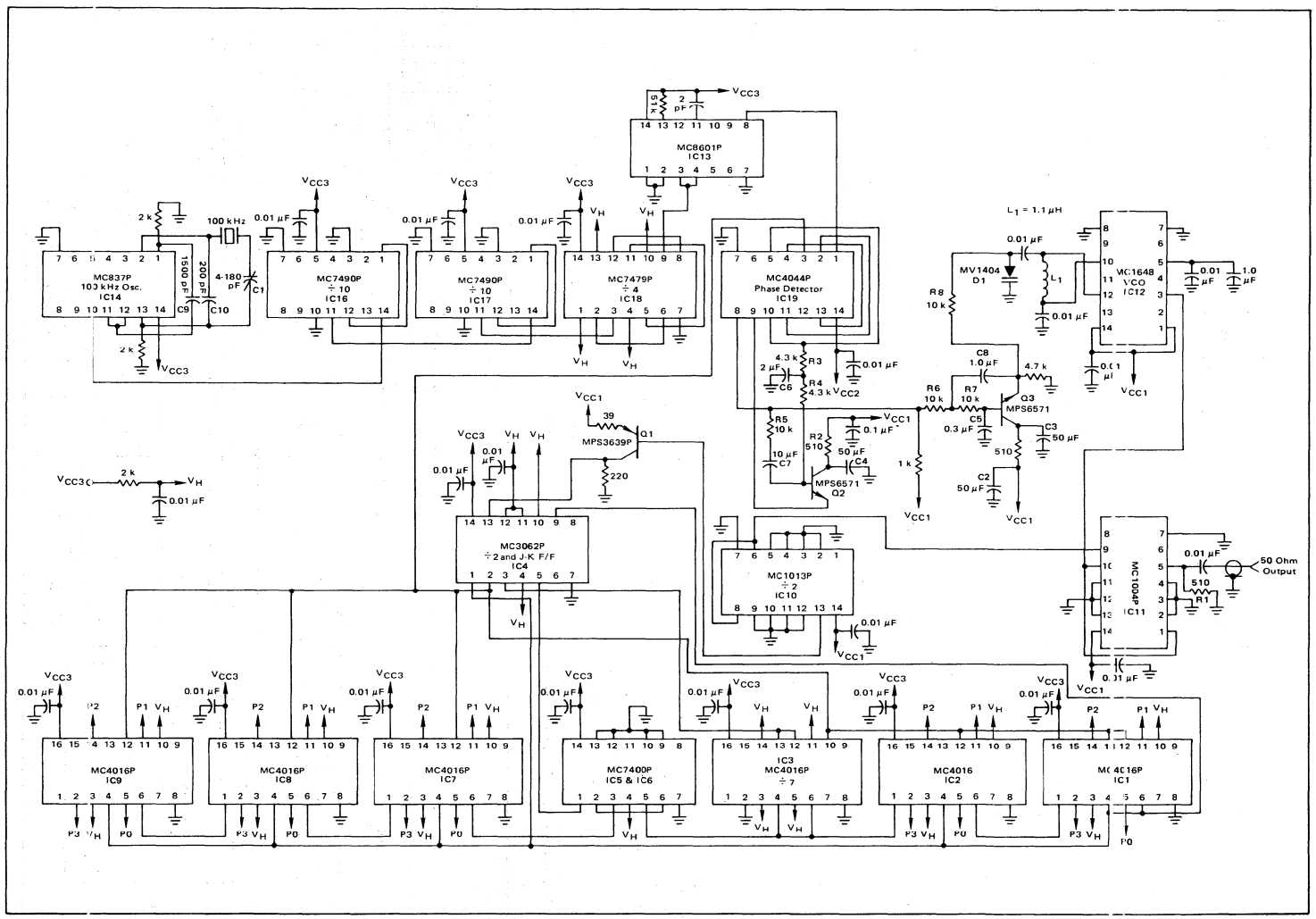


FIGURE 4 – Schematic Diagram

reference frequency feed-through energy and consequently aids filtering. The phase detector filter is reinforced by both a RC and an active filter. These additional filters further reduce the amount of 250 Hz feed-through signal on the VCO (MC1648P) control voltage. The RC filter consists of two 4.3 k ohm resistors and a 2 μF capacitor. The active filter utilizes a transistor (MPS6571) operated in the grounded collector configuration. Associated components in the active filter are two 10 k ohm resistors, a 1.0 μF capacitor and a 0.3 μF capacitor. The attenuation of the active filter (2 pole Butterworth) at 250 Hz is approximately 50 dB with the corner frequency set at 25 Hz. Details of the active filter design are provided in Appendix A.

The input reference signal to the phase detector is compared with the output of the counter chain. At lock this comparison is both phase and frequency coherent. The resultant error signal, after filtering, provides the required dc correction voltage to the VCO. Details on circuit design are provided in Appendix B. The theoretical considerations for selecting the loop parameters (see Figure 5) are explained in the References 1, 2 and 3.

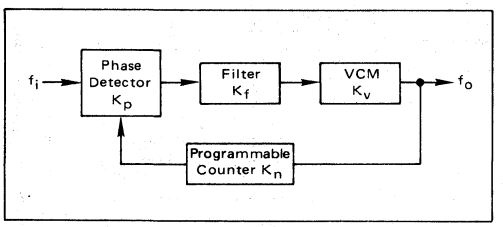


FIGURE 5 – Phase Locked Loop Circuit Parameters

The remaining digital ICs provide the required ADF local oscillator frequency range for a 10.7 MHz IF frequency. For example, when the BCD switches are set to 1620 (1620 kHz) the actual output frequency is 12.32 MHz.

The 10.7 MHz offset is provided in two sections. The 10 MHz offset is obtained by fixed-programming the last down counter IC9 (see Figure 6). For convenience, a re-labeled thumb-wheel switch was used (BCD complement). The labeling of this switch (IC9) is such that the actual programming is one more than the indicated value. Therefore, for 1620 kHz, the actual switch position is 01620, rather than 11620.

The remaining 0.7 MHz offset is provided by a J-K flip-flop, (IC4, which is 1/2 of MC3062P), two gates (IC5 and IC6) and a fixed-programmed down counter (IC3). The later is programmed for a count of 7. When this unit has counted down, the NAND gate (IC6), previously inhibited by the J-K flip-flop (IC4), is enabled. The NAND gate (IC6) enables the reamining counters, minus the first 700 pulses, thus providing the 0.7 MHz offset.

PROGRAMMING

Thumb-wheel switches are utilized to program the synthesizer. These switches program the MC4016P down counters labeled IC1, IC2, IC7, IC8 and IC9 (see Figure 5). As previously explained, IC9 utilizes a re-labeled switch, but may be fixed-programmed. Actually, since IC8 is either programmed for a 1 or 0, a simple switch can also be utilized here.

Either a BCD or BCD complement switch can be utilized for the counters. Examples of how each type is wired is shown in Figure 7.

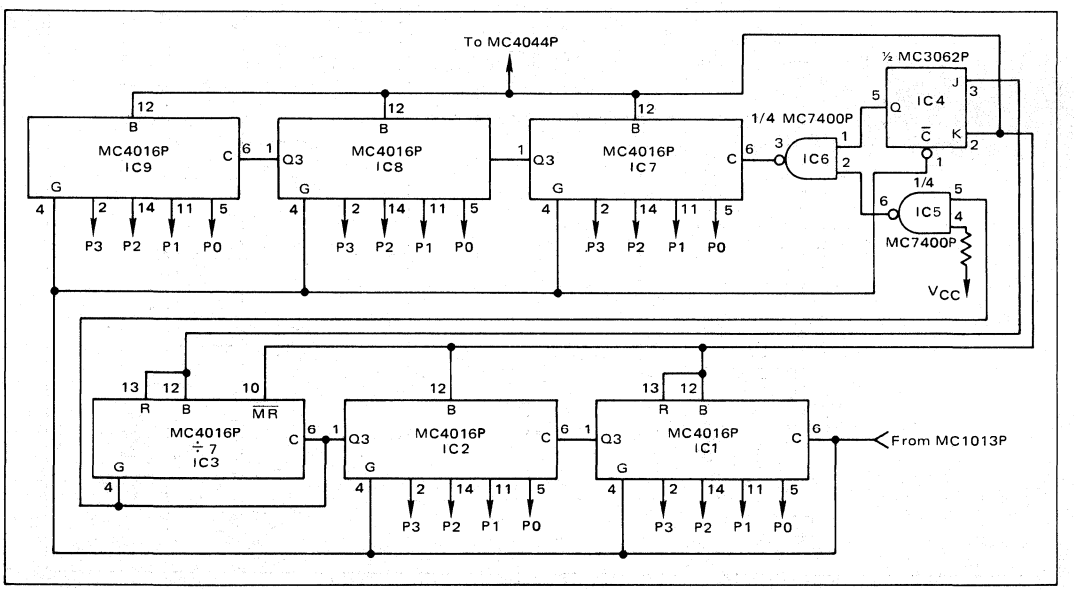


FIGURE 6 – Simplified Logic Diagram

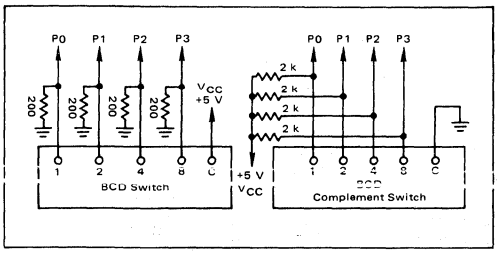


FIGURE 7 – Wiring Diagram of Thumbwheel Switches

TROUBLE-SHOOTING

No significant difficulty is anticipated in making the synthesizer operational. However, since trouble-shooting a phase-lock-loop synthesizer can be especially burdensome on the unexperienced, a brief procedure is outlined.

Initially, the thumb-wheel switches should be set for a midband frequency of 1 MHz. The switch positions should be 11000. These settings assume that five thumb-wheel switches are used. Also, switch IC9 is assumed to be in the actual "1" position. If this switch (IC9) was re-labeled as previously suggested, the setting would be "0", giving the setting of 01000. As a precaution, at least a few minutes warm-up time should be allowed for the oscillator to stabilize.

If the loop does not lock, a trouble-shooting procedure must be initiated. Generally, a good place to start is to examine the VCO. The VCO should "free run" at approximately the desired frequency, for a dc control voltage of about 1-2 volts (dc). Removing the MC4044P and externally applying 1.6 Vdc from a high resistance source (such as 10 k ohm) to the tuning diode should result in an output frequency of 11.7 MHz. Making the VCO operational will greatly facilitate checking out the digital logic.

With the VCO operational, the pre-scaler IC, translators and isolators can be checked. For instance, with a 11.7 MHz signal from pin 3 of the MC1648P, an output signal of 11.7 MHz should appear at the BNC connector (pin 5 of the MC1004P) and the input to the MC1013P (pin 8). The MECL logic levels are 3.3 V to 4.0 V. Since the MC1013P divides by 2, the frequency at pin 13 should be approximately 5.85 MHz. This signal should be translated by the MPS3639 to TTL logic levels (levels of approximately 0.5 V and 3.5 V). The input signal to pin 13 of the MC3062P is also 5.85 MHz. Since one-half of the MC3062P is a divide-by-2, the signal at pin 9 is 2.95 kHz. This signal should be at pin 6 of IC1 (see Figure 6).

The next step is to determine if the 100 kHz crystal controlled oscillator is operating. Once this oscillator is operational, the ICs prior to the MC4044P can be individually examined to determine if each is properly dividing down the 100 kHz as shown in Figure 4.

The signal into the phase detector (pin 1) should be a 250 Hz pulse train with approximately a 200 μs pulse width. This pulse width can be adjusted by varying the 50 k ohm resistor and 2 pF capacitor of the MC8601P.

The next step is to trouble-shoot the digital logic circuitry. As a prerequisite, it is recommended that each IC socket be visually examined to determine if solder connections have been made. In addition, all pins that are grounded should be checked with a VOM at the IC pin and not the socket. Each pin that is tied "high" should also be verified at the IC pin.

Initially, each MC4016P should be checked in position IC1. The other logic functions IC2, IC3, IC5, IC6, IC7, IC8 and IC9 should be removed for this check. With approximately a 2.925 kHz signal at pin 6 (and pin 4) of IC1, the output at pin 12 should be determined by the switch programming IC1. For instance, if the BCD complement switch is set to 4, the output frequency at pin 12 should be 0.73125 kHz. Each state (0-9) of each MC4016P should be verified in socket IC1. A little extra time expended in this initial checkout of the counter chain may save a great deal of vexation later while a shortcut may produce extra hours of trouble shooting time.

Before concluding that a counter is defective, the associated thumb-wheel switch wiring and IC1 connections should be checked. It may be necessary to disconnect the thumb-wheel switch and fix-program IC1 to determine if the problem is in the switch or socket wiring.

With each counter verified and position IC1 checked out, the next check is IC2. The counter in IC1 should be removed and placed in IC2. A short-wire jumper can be connected between pin 6 of IC1 and pin 6 of IC2. Again each state of one counter should be checked in socket IC2. Next a short wire should be placed from pin 6 of IC2 to pin 6 of IC7. The MC4016P would now be moved to IC7. Likewise IC8 and IC9 should be checked for each counter state.

The remaining counter IC3 should be checked to determine if it is dividing by 7. A short wire can be used to connect pin 6 of IC1 to pin 6 of IC3. The output signal of pin 12 (IC3) should be approximately 0.418 kHz. This test is of course with the other MC4016P counters removed. In addition, the MC4016P should be plugged in IC3 with pin 10 bent out to simulate pin 10 tied "high".

The remaining ICs in the feedback path (MC7400P and the MC3062P) can be first checked visually and then logically. That is, the MC3062P can be checked out against a J-K truth table.

With the feedback loop operational and the rest of the circuit restored to that shown in Figure 1, the loop should lock. If it doesn't, the remaining portion of the circuit, consisting of the MC4044P and additional filters, must be checked out.

Although the operation of MC4044P may appear complicated, several quick checks can be made to expose a problem. For example, if the frequency at pin 3 is higher than the reference signal at pin 1, then a pulse train will appear at pin 2. Likewise if pin 3 is lower in frequency than pin 1, a pulse train appears on pin 13 and pin 2 remains high. This is perhaps an over simplified test, but nevertheless a necessary requirement of the MC4044P. A simple way to perform this test is to use the 250 Hz refer-

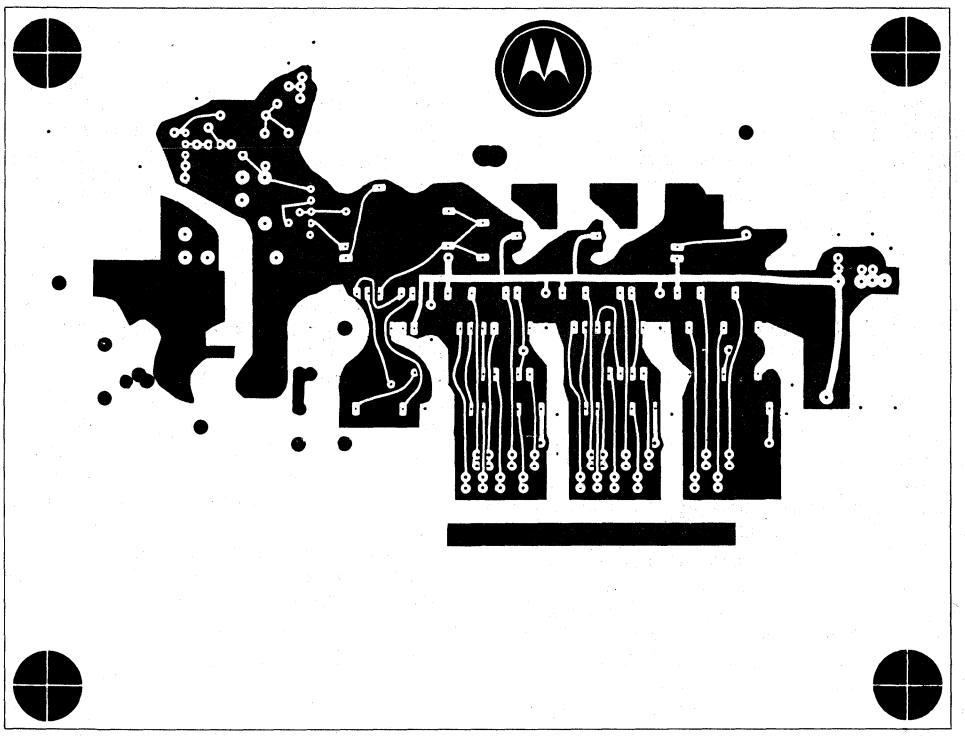


FIGURE 8 – Top of P.C. Board

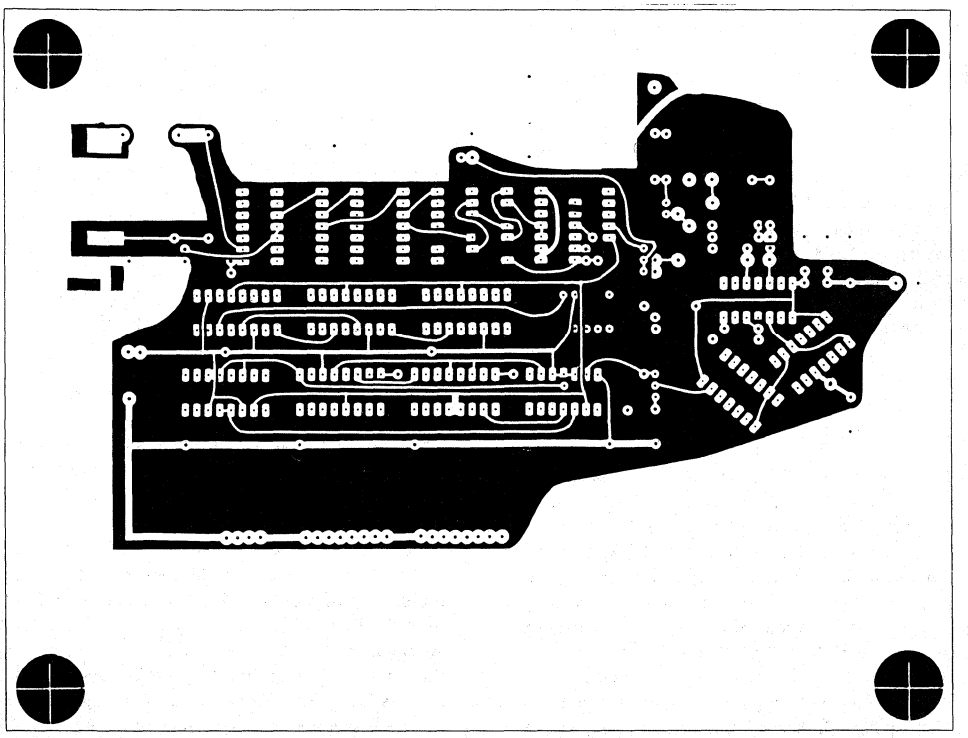


FIGURE 9 – Bottom of P.C. Board

ence signal as shown in Figure 4. Pin 3 of the MC4044P can be bent out before plugging into the socket and a pulse generator can be attached to supply the variable frequency reference to pin 3. Pin 8 of the MC4044P can be examined to determine if the dc voltage is of the correct magnitude. This voltage is determined by the frequency of the signal at pin 3. For instance, if pin 3 is lower in frequency than pin 1 (250 Hz), pin 8 should be at approximately +2.1 Vdc. If pin 3 is higher in frequency (than pin 1) then pin 8 should be approximately 0.7 Vdc.

An additional check may be made to determine if the 250 Hz reference signal is being attenuated properly. With the loop locked, there is approximately 250 mVp-p of 250 Hz signal on pins 5 and 10 of the MC4044. There is correspondingly approximately 10 mVp-p at pin 9 and 30 mVp-p at pin 8. The 250 Hz signal at the tuning diode (MV1404) is in the noise at 10 μV.

POWER SUPPLY REQUIREMENTS

Figure 4 indicates three separate, regulated positive 5 Vdc supplies (V_{CC1}, V_{CC2} and V_{CC3}). One supply is for the phase detector only, another for the VCO and filters and the third for the digital ICs. Simply connected all three supplies together will not result in the magnitude of 250 Hz rejection previously described. One solution to this problem is to operate at a single higher voltage and use RC decoupling networks to isolate each separate V_{CC} to achieve isolation. The current drain of V_{CC1}, V_{CC2} and V_{CC3} are 65 mA, 20 mA and 460 mA respectively.

PERFORMANCE

The frequency synthesizer was tested with three separate regulated supplies operated at +5 Vdc. The output frequency will vary between 10.9 MHz and 12.399 MHz with logic levels of approximately 3.3 and 4 Vdc. This produces an output signal at the BNC connector of approximately 0.7 volt p-p across 50 ohms. The wave form before filtering approximates a square wave.

The frequency spectrum from 10 kHz to the output frequency is -60 dB down or greater. The frequency spectrum from the carrier to 2 kHz is also noise with a floor of approximately -40 dB at 75 Hz out from the carrier and -50 dB, 300 Hz out from the carrier. The 250 Hz reference signal feed-through is not discernible.

The lock-up time is typically 0.5 s for down-frequency steps and 1.0 s for up-frequency steps.

CIRCUIT MODIFICATIONS

The basic circuit shown may be used for output frequencies up to 40 MHz without circuit board changes. This frequency corresponds to a maximum input frequency to IC1 of about 10 MHz. The circuit shown can be further optimized for 10.7 MHz performance by omitting the MC1013P (divide-by-2) and re-wiring the MC7479P for a divide-by-2. This change will increase the reference frequency to 500 Hz and should decrease the noise floor to approximately -60 dB.

CIRCUIT CONSTRUCTION

The circuit shown in Figure 5 was constructed on two-sided printed circuit board. The circuit board mask for both sides is shown in Figures 8 and 9. A photograph of the top and bottom of the circuit board showing component locations is given in Figure 10.

CONCLUSION

This report describes a frequency synthesizer adequate for the local oscillator function in ADF equipment. Higher frequency capability is available without adding more ICs. Detailed printed circuit board masks, component location diagrams and a trouble-shooting description is included to facilitate construction.

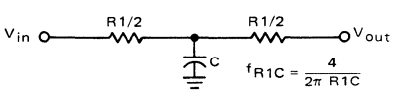
BIBLIOGRAPHY

1. Jon DeLaune, MTTL and MECL Avionic's Digital Frequency Synthesizer, Motorola Semiconductor Products Inc., Application Note AN-532A.
2. Garth Nash, Phase-Locked Loop Design Fundamentals, Motorola Semiconductor Products Inc., Application Note AN-535.
3. Richard Brubaker and Garth Nash, A New Generation of Integrated Avionic Synthesizers, AN-553.

6

APPENDIX A

Two additional filters, an RC filter and an active filter are used to reduce the 250 Hz reference feed-through. The RC filter is diagramed below:



To insure reasonable isolation with the phase-lock loop, the corner frequency of this filter and the active filter were set at 25 Hz or approximately ten times the loop bandwidth.

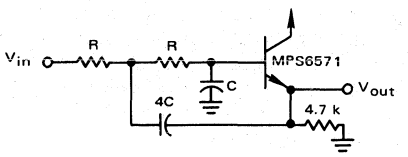
$$f_{R1C} = 25 \text{ Hz.}$$

with R1 = 10 k as will be shown in Appendix B,

$$C = 2.3\ \mu F \text{ from } f_{R1C} = \frac{4}{2\pi\ R1C}$$

The actual value used was 2 μF

The corner frequency of the active filter is also 25 Hz. A MPS6571 is operated grounded collector to provide high input impedance. The component values for this filter



are calculated from:

$$f \approx \frac{1}{4\pi RC}$$

Thus letting R = 10 k, f = 25 Hz,

$$C \approx 0.3\ \mu F$$
$$4C \approx 1\ \mu F$$

APPENDIX B

PHASE-LOCK LOOP FILTER DESIGN

The following example describes the design procedure for obtaining the phase-lock loop filter components shown in Figure 1. The following equations are from Reference 2.

$$N_{max} = \frac{1}{K_n} = \frac{f_{max}}{f_{step}}$$

$$\omega_n t = x$$

$$R1C = \frac{0.5\ K_p\ K_v}{\omega_n^2\ N_{max}}$$

$$R2 = \frac{2\zeta}{C\omega_n}$$

$$\omega_{3\ dB} = \omega_n \left[1 + \zeta^2 + \sqrt{2 + 4\zeta^2 + 4\zeta^2}\right]$$

The above parameter values are:

1. t = 450 ms (chosen)
2. $K_p \cong 0.111$ V/rad (MC4044 data sheet)
3. $\zeta = 0.5$ (chosen)
4. $K_v \cong 9.5 \times 10^6$ rad/s/V (measured value, see Reference 1)
5. x = 4.5 (see Figure 6, Reference 2)
6. f_{max} = 1699 kHz + 10.7 MHz
7. f_{step} = 250 Hz

Hence, solving for N_{max}, using the above values:

$$N_{max} = \frac{f_{max}}{f_{step}} = \frac{(1699\ kHz + 10.7\ MHz)}{250\ Hz}$$

$$= 4.95 \times 10^4$$

Next, solving for ω_n,

$$\omega_n = \frac{x}{t} = \frac{4.5}{450\ ms}$$

$$= 10\ rad/s$$

Now, solving for R1 by choosing a value of C equal to 10 μF we have:

$$R1C = \frac{0.5\ K_p\ K_v}{\omega_n^2\ N_{max}}$$

$$\text{or } R1 = \frac{(0.5)(0.111)(9.5 \times 10^6)}{(10)^2(4.95 \times 10^4)\ (10 \times 10^{-6})}$$

$$= 10.65\ k\Omega$$

Solving for R2:

$$R2 = \frac{2\zeta}{C\omega_n}$$

$$R2 = \frac{(2)(0.5)}{(10\ \mu F)(10)}$$

$$R2 = 10\ k\Omega$$

Finally solving for the bandwidth:

$$\omega_{(-3dB)} = \omega_n \left[1 + \zeta^2 + \sqrt{2 + 4\zeta^2 + 4\zeta^4}\right]$$

choosing $\zeta = 0.5$

$$\omega_{(-3dB)} = (\omega_n)(1.8)$$

$$\text{thus } f_{(-3dB)} = \frac{(\omega_n)(1.8)}{2\pi}$$

$$= 2.87\ Hz.$$

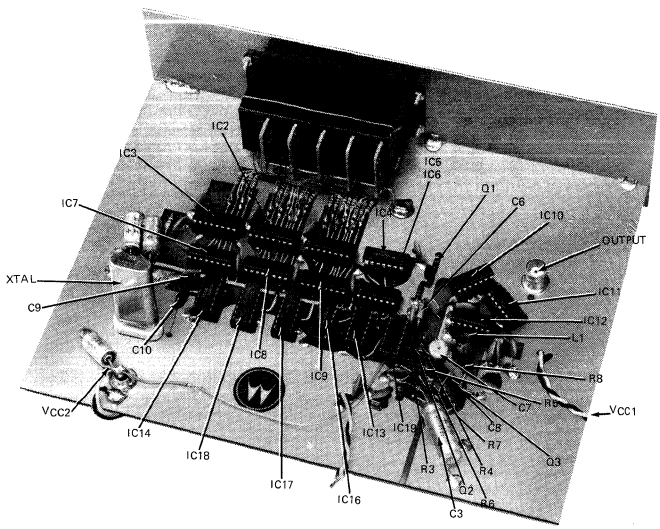


FIGURE 10A – Photograph of Top of Board

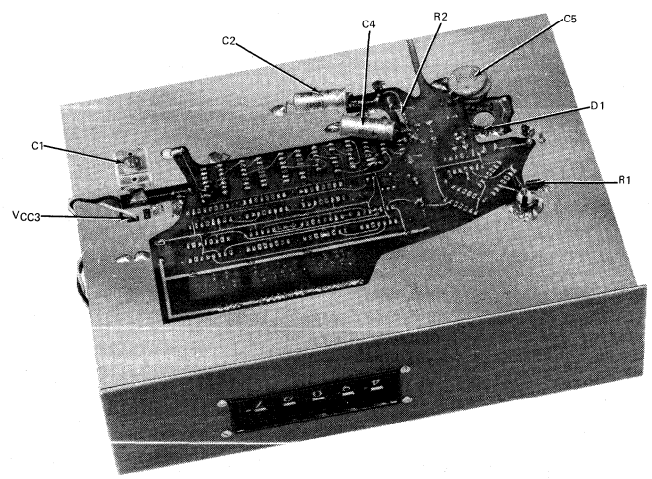
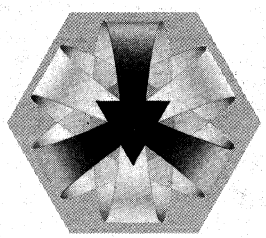


FIGURE 10B – Photograph of Bottom of Board

PACKAGING



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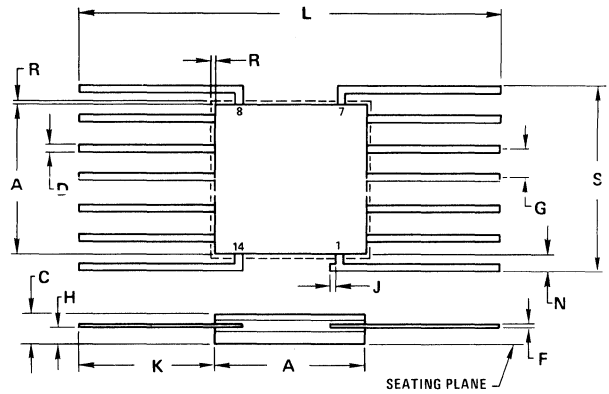
CASE 607

TO-86

F Suffix
Ceramic Package

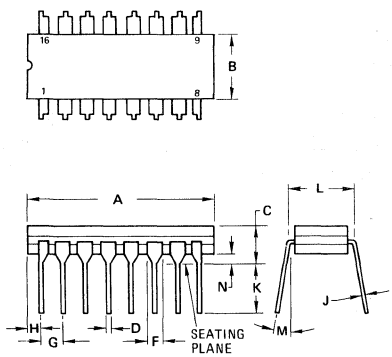


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
C	0.76	1.78	0.030	0.070
D	0.33	0.48	0.013	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.30	0.89	0.012	0.035
J	–	0.38	–	0.015
K	6.35	9.40	0.250	0.370
L	18.80	–	0.740	–
N	0.25	–	0.010	–
R	–	0.38	–	0.015
S	7.62	8.38	0.300	0.330

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NOT CONNECTED
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NOT CONNECTED
12. EMITTER
13. BASE
14. COLLECTOR

CASE 620

L Suffix
Ceramic Package



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.99	0.245	0.275
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.31	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.37	7.87	0.290	0.310
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

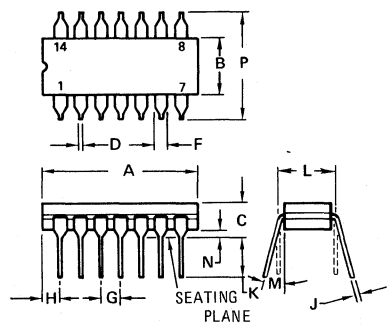
NOTES:

DIM "L" TO CENTER OF LEADS
WHEN FORMED PARALLEL.

CASE 632

TO-116

L Suffix
Ceramic Package



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.8	19.9	0.660	0.785
B	5.59	7.11	0.220	0.280
C	–	5.08	–	0.200
D	0.381	0.584	0.015	0.023
F	0.77	1.77	0.030	0.070
G	2.54 BSC		0.100 BSC	
J	0.203	0.381	0.008	0.015
K	2.54	–	0.100	–
L	7.62 BSC		0.300 BSC	
M	–	15°	–	15°
N	0.51	0.76	0.020	0.030
P	–	8.25	–	0.325

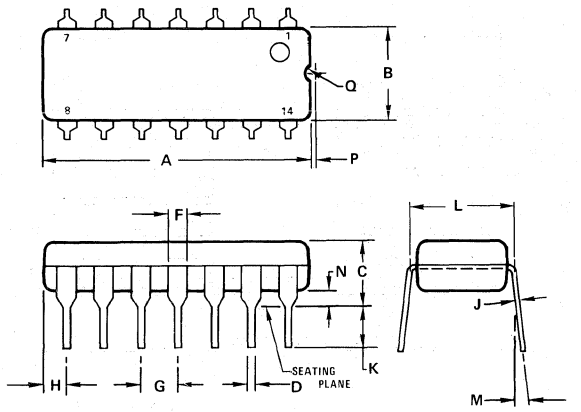
All JEDEC dimensions and notes apply.

NOTE:

DIMENSION "L" TO CENTER OF
LEADS WHEN FORMED PARALLEL.

CASE 646

P Suffix
Plastic Package

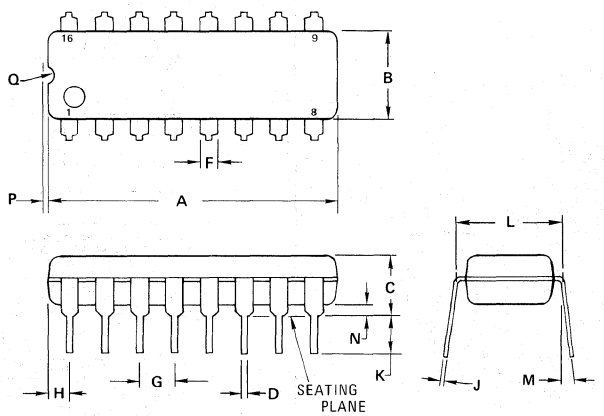


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10^0	–	10^0
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

CASE 648

P Suffix
Plastic Package



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10^0	–	10^0
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

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Closing The Loop

After you have examined the Phase-Locked Loop Data Library you may wish to evaluate certain devices or prototype a system. The following schedule is intended to furnish cost information as of May 1, 1973. Semiconductor prices vary, particularly new product offerings. Increased usage through widespread product acceptance usually results in price reductions. For current prevailing prices at the time of your application we suggest you contact your local franchised Motorola distributor or sales office.

DEVICE	UNIT PRICE (1-99)	UNIT PRICE (100-999)
MC4024P	$ 2.60	$ 2.20
MC4044P	2.60	2.20
MC1648P	3.75 *	2.50
MC1658P	4.42 *	2.95
MC12000L	7.50 *	5.00
MC12012L	19.50 *	13.00
MC12014L	6.40 *	4.25
MC74416P	6.50	5.50
MC74418P	6.50	5.50
MC4023P	4.20	3.50
MC7490P	2.30 *	1.50
MC1678L	64.80 *	43.20
MC1690L	55.00 *	45.00
MC10136L	17.79 *	14.23
MC10137L	17.79 *	14.23
MC14017CP	4.61	3.82
MC14040CP	5.89	4.86
MC14510CP	6.91	5.72
MC14516CP	6.91	5.72
MC14518CP	6.91	5.72
MC14520CP	6.91	5.72
MC14522CL	7.95	6.60
MC14526CL	7.95	6.60

**1—24 quantity*

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